Acromag®

Series IP480 Industrial I/O Pack
Six & Two 16-Bit Counter/Timer Modules

USER'S MANUAL

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8500-558-E05H001

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IMPORTANT SAFETY CONSIDERATIONS

It is very important for the user to consider the possible adverse effects of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where economic property loss or human life is involved. It is important that the user employ satisfactory overall system design. It is agreed between the Buyer and Acromag, that this is the Buyer's responsibility.

1.0 GENERAL INFORMATION

The Industrial I/O Pack (IP) Series IP480 module provides support for up to six channels of multifunction counter/timer operation. The IP480 provides 6 different counter modes with internal or external triggering and clocking, plus interrupt support. This model may be configured as an event counter, a waveform generator, a watchdog timer, or a pulse-width or period monitor. Combinations of up to six 16-bit, or three 32-bit counter/timer (C/T) functions may be configured for interface to the VMEbus or ISAbus, according to your carrier board. Four units may be mounted on a single carrier board to provide up to twenty-four 16-bit counter/timer functions per system slot.

The IP480 is available with two or six 16-bit counter/timers, in standard and extended temperature range models as follows:

MODEL	COUNTER/TIMERS, TEMPERATURE RANGE
IP480-2	Two 16-bit (or one 32-bit) Counter/Timers, 0 to 70°C
IP480-6	Six 16-bit (or three 32-bit) Counter/Timers, 0 to 70°C
IP480-2E	Two 16-bit (or one 32-bit) Counter/Timers, -40 to 85°C
IP480-6E	Six 16-bit (or three 32-bit) Counter/Timers, -40 to 85°C

The IP480 utilizes state of the art Surface-Mounted Technology (SMT) to achieve its wide functionality and is an ideal choice for a wide range of industrial I/O applications that require a high-density, highly reliable, high-performance counter/timer interface at a low cost.

KEY IP480 FEATURES

- **High Counter/Timer Density** - Provides programmable monitor and control of up to six 16-bit counter/timer functions, or three 32-bit functions. Four units mounted on a carrier board provide up to 24 counter/timer functions in a single VMEbus or ISAbus (PC/AT) system slot.
- **Extended Temperature Range Performance** - "E" suffix units support the extended ambient temperature range of -40°C to +85°C.
- **Output Waveform Generation** - The IP480 may generate up to six pulse or square wave outputs. Pulse waveforms may be generated continuously, or one time (one-shot mode). Square waveforms are generated continuously.
- **16/32-Bit Input Event Counters** - The IP480 can be configured to count input pulses or events to 16-bit count values (on up to 6 inputs), or 32-bit count values (on up to 3 inputs). Support for event interrupt generation and output control is also provided.

- **Watchdog Timer** - Six 16-bit or three 32-bit countdown timers are possible with output control and optional interrupt generation (IP480-6 units). IP480 units also include watchdog timer control of electro-mechanical SPDT (1 Form C) relay contacts.
- **Pulse-Width or Periodic Rate Measurement -** The IP480 can be configured to measure pulse-width or waveform period.
- **Programmable Interface Polarity** - The polarities of the counter's external trigger, input, and output pins are programmable for active high or low operation.
- **Interrupt Support** - The IP480 can be configured to generate interrupts for several different conditions: watchdog timer time-out, event count complete, pulse-width or periodic rate measurement complete, or waveform cycle complete.
- **Easy to Program** - Most counter configuration is done through a single register and no more than three registers need to be written to initiate any counter/timer function. These include the Counter Constant Register, Counter Control Register, and Interrupt Vector Register. If triggered internally, then a fourth register, the Trigger Control Register, will need to be written to start the function.
- **Internal or External Triggering** - A software or hardware trigger is selectable to initiate waveform generation, watchdog countdown, event counting, or pulse-width or periodic-rate measurement.
- **Internal or External Clock Support** - Counter functions may use internally generated 1MHz, 4MHz, and 8 MHz clocks, or externally supplied clocks up to 3.5MHz (external clocks are internally synchronized to the IP clock).
- **High Current/High Voltage Digital Outputs** - Digital timer outputs are the open drains of N-channel mosfets and can sink up to 250mA each. Outputs are rated to 60V DC and include "snubber" clamp protection built-in.
- **SPDT Relay Outputs Included** - IP480 units include separate isolated electro-mechanical SPDT (1 Form C) watchdog timer outputs rated to 125VAC and 1A.
- **Flexible Output Drive Capability** - The open drain pullups at the timer outputs are installed in sockets on the board for ease of removal or replacement when adjusting the output drive capability. Additionally, they can be jumpered to the external supply input pin (field connector P2 pin 1), or the +5V board supply for flexible level adjustment.
- **Built-In Output Clamp Diode** - The open-drain outputs of this module include built-in "snubber" or clamp diodes for added protection when driving inductive loads.
- **No Configuration Jumpers or Switches** - All configuration is performed through software commands with no internal jumpers to configure or switches to set. However, a jumper is provided to select where to strap the output drain pullups (to the internal +5V or to an external field supply).

INDUSTRIAL I/O PACK INTERFACE FEATURES

- **High density -** Single-size, industry standard, IP module footprint. Four units mounted on a carrier board provide up to 24 16-bit counter/timer functions in a single system slot. Both VMEbus and ISAbus (PC/AT) carriers are supported.
- **Local ID** - Each IP module has its own identification information space accessed via data transfers in the "ID Read" space.
- **8-bit or 16-bit I/O** - Port register Read/Write is performed through 8-bit or 16-bit data transfer cycles in the IP module I/O space.
- **High Speed With Only 1 Wait State** - Access times for data transfer cycles are described in terms of "wait" states--1 wait state is required for most read and write operations of this model, except for serving the interrupt vector which takes 0 wait states. See Specifications section for detailed information.

SIGNAL INTERFACE PRODUCTS

(See Appendix for more information on compatible products)

This IP module will mate directly to any industry standard IP carrier board (including Acromag AVME9630/9660 3U/6U non-intelligent VMEbus carrier boards). Additionally, PC carrier boards are also supported (see Acromag Model APC8610). A wide range of other Acromag IP modules are also available to serve your signal conditioning and interface needs.

Note: Since all connections to field signals are made through the carrier board which passes them to the individual IP modules, you should consult the documentation of your carrier board to ensure compatibility with the following interface products.

Cables:

Model 5025-551-X (Shielded Cable), or Model 5025-550-X (Non-Shielded Cable): A Flat 50-pin cable with female connectors at both ends for connecting AVME9630/9660, or other compatible carrier boards, to Model 5025-552 termination panels. The unshielded cable is recommended for digital I/O, while the shielded cable is recommended for optimum performance with precision analog I/O applications. The "-X" suffix of the model number denotes the length in feet.

Termination Panels:

Model 5025-552: A DIN-rail mountable panel that provides 50 screw terminals for universal field I/O termination. Connects to Acromag AVME9630/9660, or other compatible carrier boards, via flat 50-pin ribbon cable (Model 5025-550-X or 5025-551-X).

Transition Module:

Model TRANS-GP: This module repeats field I/O connections of IP modules A through D for rear exit from a VMEbus card cage. It is available for use in card cages which provide rear exit for I/O connections via transition modules (transition modules can only be used in card cages specifically designed for them). It is a double-height (6U), single-slot module with front panel hardware adhering to the VMEbus mechanical dimensions, except for shorter printed circuit board depth. It connects to Acromag Termination Panel 5025-552 from the rear of the card cage, and to AVME9630/9660 boards within the card cage, via flat 50-pin ribbon cable (cable Model 5025-550 or 5025-551).

INDUSTRIAL I/O PACK SOFTWARE LIBRARY

Acromag provides an Industrial I/O Pack Software Library diskette (Model IPSW-LIB-M03, MSDOS format) to simplify communication with the board. Example software functions are provided for both ISAbus (PC/AT) and VMEbus applications. Software functions are written in the "C" programming language and can be linked to your application. For more details, refer to the "README.TXT" file in the root directory on the diskette and the "INFO480.TXT" file in the appropriate "IP480" subdirectory off of "\VMEIP" or "\PCIP", according to your carrier.

INDUSTRIAL I/O PACK OLE CONTROL SOFTWARE

Acromag provides a software diskette of Industrial I/O Pack Object Linking and Embedding (OLE) drivers for Windows 95 and Windows NT compatible application programs (Model IPSW-DVR-OLE-PC, MSDOS format). This software provides individual drivers that allow Acromag I/O Packs and the APC8610 carrier to be easily integrated into Windows application programs, such as Visual C++, Visual Basic, etc. The OLE controls provide a high-level interface to Acromag I/O Packs, eliminating the need to perform low-level reads/writes of registers, and the writing of interrupt handlers—all the complicated details of programming are handled by the OLE controls. These functions are intended for use in conjunction with the Acromag APC8610 ISAbus (PC/AT) carrier and consist of a Carrier Configuration Program, and APC8610 OLE control, and an OLE control for each Acromag I/O Pack model.

2.0 PREPARATION FOR USE

UNPACKING AND INSPECTION

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection. For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

CAUTION
SENSITIVE ELECTRONIC DEVICES
DO NOT SHIP OR STORE NEAR STRONG ELECTROSTATIC, ELECTROMAGNETIC MAGNETIC OR RADIOACTIVE FIELDS

This board is physically protected with packing material and electrically protected with an anti-static bag during shipment. However, it is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

The board utilizes static-sensitive components and should only be handled at a static-safe workstation.

CARD CAGE CONSIDERATIONS

Refer to the specifications for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the carrier board, plus the installed IP modules, within the voltage tolerances specified.

IMPORTANT: Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.

The dense packing of the IP modules to the carrier board restricts air flow within the card cage and is cause for concern. Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

BOARD CONFIGURATION

Power should be removed from the board when installing IP modules, cables, termination panels, field wiring, or output pullups. Refer to Mechanical Assembly Drawing 4501-434 and your IP module documentation for configuration and assembly instructions. Model IP480 I/O boards normally have no hardware jumpers or switches to configure. All configuration is done through software commands. Likewise, no external wiring is required to cascade channels for 32-bit functionality. However, a supply jumper is included for strapping the output drain pullups to the internal +5V supply (default position), or to the external field supply pin (P2 Pin 1). Likewise, an output open-drain pullup SIP resistor (packaged separately) must be installed (see below).

Pullup Resistor Installation, Replacement, & Removal

The timer outputs are the open-drains of N-channel mosfets with a common source connection. These drains are pulled up through resistor SIP R2 installed in socket X1. The pullup supply may be +5V on board, or an external supply up to 60V, by programming the external supply jumper (see below). Note that 470Ω resistor SIP is packaged separate from the module. A 4.7KΩ Resistor Pack is installed in socket X1 for proper output operation (see Drawing 4501-610). Socket X1 may accommodate a common 6, 7, or 8 resistor SIP, or external pullups may be employed. It is important that the power through the SIP resistors provided be limited to no more than 0.15 Watts per resistor. If the output pullups are using an external supply at P2, then the pullup value must be adjusted with power limitations in mind. To prevent damage to the SIP resistors, do not use an external supply greater than 26V with the 4.7KΩ SIP installed, or 8V with the 470Ω SIP installed. Raise the value of this resistor for use with greater external supply voltages. Note that the output response time is also strongly dependent on this resistor value. Lower pullup values will increase the output speed, but power dissipation will also increase and limit maximum permissible external supply levels.

External Supply Jumper Placement

A jumper (J1) is provided on board to connect the counter open-drain output pullups to the +5V board supply (default position), or to an external supply tied to the P2 interface at pin 1 (refer to Drawing 4501-610). This provides flexibility for adjusting the output level and drive capability. Place jumper J1 between P3 pins 2 & 3 for the +5V pullup supply (default position), or P3 pins 1 & 2 for external supply pullup. An external supply must be limited to 60V or less. Likewise, do not exceed 0.15W per pullup resistor at each output drain, or damage to SIP resistor R2 will result.

CONNECTORS

IP Field I/O Connector (P2)

P2 provides the field I/O interface connections for mating IP modules to the carrier board. P2 is a 50-pin female receptacle header (AMP 173279-3 or equivalent) which mates to the male connector of the carrier board (AMP 173280-3 or equivalent). This provides excellent connection integrity and utilizes gold-plating in the mating area. Threaded metric M2 screws and spacers are supplied with the module to provide additional stability for harsh environments (see Mechanical Assembly Drawing 4501-434). The field and logic side connectors are keyed to avoid incorrect assembly.

P2 pin assignments are unique to each IP model (see Table 2.1 below) and normally correspond to the pin numbers of the field I/O interface connector on the carrier board (you should verify this for your carrier board).

Table 2.1A: IP480 Field I/O Pin Connections (P2) – 16-Bit Counter Configurations

Pin Description		Number	Pin Description	Number
External Supply		1	Common	30
Common		2	No Connection	31
C	Trigger1	3	**RELAY 1:**	
N	Input1	4	1A (N.O.)	32
T	Clock1	5	1C	33
1	Output1	6	1B (N.C.)	34
Common		7		
C	Trigger2	8	**RELAY 2**	
N	Input2	9	2A (N.O.)	35
T	Clock2	10	2C	36
2	Output2	11	2B (N.C.)	37
C	Trigger3	12	**RELAY 3**	
N	Input3	13	3A (N.O.)	38
T	Clock3	14	3C	39
3	Output3	15	3B (N.C.)	40
Common		16		
C	Trigger4	17	**RELAY 4**	
N	Input4	18	4A (N.O.)	41
T	Clock4	19	4C	42
4	Output4	20	4B (N.C.)	43
C	Trigger5	21	**RELAY 5**	
N	Input5	22	5A (N.O.)	44
T	Clock5	23	5C	45
5	Output5	24	5B (N.C.)	46
Common		25		
C	Trigger6	26	**RELAY 6**	
N	Input6	27	6A (N.O.)	47
T	Clock6	28	6C	48
6	Output6	29	6B (N.C.)	49
			Shield	50

I/O channels of this module are divided into 6 functional counter/timer (C/T) groups as shown in Table 2.1A. Note that for some C/T functions, 32-bit functionality is obtained using two consecutive 16-bit C/T groups as illustrated in Table 2.1B. Each group shares a common signal connection with each other. Thus, IP480 units are generally non-isolated, except for the watchdog timer output relay contacts. Isolation is provided between the individual relays and between each relay and the IP logic. Refer to Drawing 4501-611 for example I/O connections.

The polarities of the counter output, input, and trigger pins are programmable as active high or low. Outputs are the open-drains of N-channel mosfets with a common source connection. Drain pullups to +5V are installed in sockets on the board. A jumper on board allows these pullups to be pulled up to the +5V IP supply (default position), or to the external supply pin (P2 Pin 1). Outputs include built-in "snubber" or clamp diodes for added protection when driving inductive loads.

Table 2.1B: IP480 Field I/O Pin Connections (P2) – 32-Bit Counter Configurations

Pin Description		Number	Pin Description	Number
External Supply		1	Common	30
Common		2	No Connection	31
	Unused	3	**RELAY 1:**	
	Unused	4	Unused	32
	Unused	5	Unused	33
	Unused	6	Unused	34
Common		7		
C	Trigger2	8	**RELAY 2**	
N	Input2	9	2A (N.O.)	35
T	Clock2	10	2C	36
2	Output2	11	2B (N.C.)	37
	Unused	12	**RELAY 3**	
	Unused	13	Unused	38
	Unused	14	Unused	39
	Unused	15	Unused	40
Common		16		
C	Trigger4	17	**RELAY 4**	
N	Input4	18	4A (N.O.)	41
T	Clock4	19	4C	42
4	Output4	20	4B (N.C.)	43
	Unused	21	**RELAY 5**	
	Unused	22	Unused	44
	Unused	23	Unused	45
	Unused	24	Unused	46
Common		25		
C	Trigger6	26	**RELAY 6**	
N	Input6	27	6A (N.O.)	47
T	Clock6	28	6C	48
6	Output6	29	6B (N.C.)	49
			Shield	50

The SPDT electromechanical relay outputs are controlled by the watchdog timer only. The "A" contact is the Normally-Open (N.O.) contact and the B contact is the Normally-Closed (N.C.) contact. The "C" contact is the wiper/pole terminal. A brief description of each of the P2 counter/timer I/O pins is included in the following table (shaded pins are isolated):

Counter/Timer Pin Descriptions

PIN	FUNCTION
Trigger[1]	This pin is the external trigger input used to re-trigger and/or start a counter/timer operation when external triggering has been selected. For event counter operations, this signal may serve as the initial trigger to begin counting events which continues to cycle without a re-trigger. For watchdog timer operation, waveform generation, and pulse-width or period measurement, this signal may serve as the initial trigger to begin the operation, plus the re-trigger required to recycle. A minimum pulse-width of 140ns is required for the external Trigger signal. The polarity of this input pin is programmable.
Input[1]	This pin is used as a sampling input for pulse-width and periodic measurement, and the event counter input. It is also used to initiate the loading of the watchdog timer counter from the counter constant register when external loading is programmed (via bit 11 of the Counter Control Register). The active polarity of this input pin is programmable. The minimum input high or low pulse width is 140ns.
Clk[1]	When external clocking is selected, the external clock is input to this pin (3.5MHz maximum). The counter/timer is clocked on the rising edge of this signal. Internal or external clocking has no effect for the event counter function.
Out	This is an open-drain output pin tied to a pullup resistor installed in a socket on the board. A 1us pulse will be generated at this pin upon event count limit reached, or when a pulse-width or period measurement is complete. In watchdog timer mode, this pin is driven in tandem with the corresponding relay (active while countdown, inactive upon timeout). This pin is also driven while generating waveforms. The active polarity of this output pin is programmable. This pin is pulled high after a reset (default polarity is active low).
External Supply	The output pins of the counter/timers are open-drain mosfets tied to pullup resistors installed in sockets on the board. These pullups can be jumpered to +5V, or to this pin, which allows the user to adjust the output level or drive capability by providing another supply at this input. An external supply of up to 60V may be used (standard pullups removed), but should be less than or equal to 26V with the 4.7K pullups, or 8V with 470Ω pullups installed to limit the power dissipation in these resistors. Adjust pullup value higher to limit power dissipation with greater external supply voltages.
Common	This is the output common/ground connection which is also common to the output mosfet sources.
A	This is the watchdog-timer relay normally-open relay contact. A & C make contact only while the watchdog timer is counting.
C	Watchdog-timer SPDT relay wiper/pole contact.
B	This is the watchdog-timer relay normally-closed relay contact. B & C make contact while power is off, while the watchdog timer is not configured, and upon watchdog timer time-out.

Notes:

1. By default, all field inputs are not debounced. Clean, well-defined TTL or CMOS input signals are normally required for error-free operation. Limited debounce capability for the Counter Input of counters 1 and 2 can be selected via the Counter Control Register bit 12 and this will cause input pulses less than 1us in duration to be rejected (Note: This applies to input of counters 1 and 2 only, not the clock or trigger).

For 32-bit counter/timer functions, two consecutive 16-bit registers are required. Thus, only three 32-bit counters may be configured per module. The odd-numbered counter of the consecutive pairs always holds the Most-Significant Word (MSW) of the 32-bit value (counters 1, 3, & 5), the even-numbered counter holds the Least-Significant Word (LSW) of the 32-bit value (channels 2, 4, & 6). Configuration and control of the 32-bit counter/timer is obtained through the even-numbered Counter Control Registers and input signals, while the odd-numbered Counter Control Registers and inputs are ignored for 32-bit applications. Note that no external wiring is required to cascade IP480 timer/counters for 32-bit functionality.

Noise and Grounding Considerations

The counter outputs of the IP480 are the open drains of mosfets with a common source connection. Likewise, all field I/O lines of IP480 modules are not isolated from each other and they share a common connection. Thus, these lines are non-isolated between the logic and field I/O grounds since output common is electrically connected to the IP module ground. Consequently, the field I/O connections are not isolated from the carrier board and backplane. Two ounce copper ground plane foil has been employed in the design of this model to help minimize the effects of ground bounce, impedance drops, and switching transients. However, care should be taken in designing installations without isolation to avoid noise pickup and ground loops caused by multiple ground connections.

The watchdog timer output relays of the IP480 are isolated from each other and between the logic and relay field connections (all other field I/O connections are non-isolated). Consequently, the field output relay contacts are isolated from the carrier board, backplane, and each other, thus minimizing the negative effects of ground bounce, impedance drops, and switching transients for relay connections. However, care should be taken in designing installations to avoid inadvertent isolation bridges, noise pickup, isolation voltage clearance violations, equipment failure, or ground loops.

This device is capable of switching several C/T outputs at high total currents. Likewise, the nature of the IP interface is inherently inductive. The open-drain outputs of this model are protected to voltages up to 60V and include built-in clamping devices. However, when switching inductive loads, it is important that careful consideration be given to the use of external “snubber” devices to shunt the reverse emf that develops when the current through an inductor is interrupted. Filtering and bypassing at the load may also be necessary. Additionally, proper grounding with thick conductors is essential. Interface cabling and ground wiring should be kept as short as possible. The use of an interposing relay may also be desirable for isolating the load, raising the drive capability, or providing additional system protection. Please refer to Drawing 4501-611 for examples of these connections and proper output and grounding recommendations.

Because this device does not normally implement debounce on any of the counter/timer inputs (Trigger, Input, and Clock) and these inputs have a wide bandwidth, it is very important that input signals are kept clean and noise free to prevent potential errors. Well defined TTL or CMOS signal levels are preferred. When driving inputs, use of 50Ω generator outputs or a 50Ω series-coupled resistor will improve results. If noisy field input signals and erratic operation continues to occur, some consideration should be given to external filtering or wave shaping of the input signals to prevent these types of errors.

IP Logic Interface Connector (P1)

P1 of the IP module provides the logic interface to the mating connector on the carrier board and its pin assignments are standard for all IP modules according to the Industrial I/O Pack Specification (see Table 2.2). This connector is a 50-pin female receptacle header (AMP 173279-3 or equivalent) which mates to the male connector of the carrier board (AMP 173280-3 or equivalent). This provides excellent connection integrity and utilizes gold-plating in the mating area. Threaded metric M2 screws and spacers are supplied with the IP module to provide additional stability (see Drawing 4501-434 for assembly details). Field and logic side connectors are keyed to avoid incorrect assembly.

Table 2.2: Standard Logic Interface Connections (P1)

Pin Description	Number	Pin Description	Number
GND	1	GND	26
CLK	2	+5V	27
Reset*	3	R/W*	28
D00	4	IDSEL*	29
D01	5	***DMAReq0****	30
D02	6	MEMSEL*	31
D03	7	***DMAReq1****	32
D04	8	IntSel*	33
D05	9	***DMAck0****	34
D06	10	IOSEL*	35
D07	11	***RESERVED***	36
D08	12	A1	37
D09	13	***DMAEnd****	38
D10	14	A2	39
D11	15	***ERROR****	40
D12	16	A3	41
D13	17	INTReq0*	42
D14	18	A4	43
D15	19	***INTReq1****	44
BS0*	20	A5	45
BS1*	21	***STROBE****	46
-12V	22	A6	47
+12V	23	ACK*	48
+5V	24	***RESERVED***	49
GND	25	GND	50

An Asterisk (*) is used to indicate an active-low signal.
BOLD ITALIC Logic Lines are NOT USED by this IP Model.

3.0 PROGRAMMING INFORMATION

ADDRESS MAPS

This board is addressable in the Industrial Pack I/O space to monitor and control the status and configuration of up to six 16-bit counter/timers, or three 32-bit counter/timers. The I/O space may be as large as 64, 16-bit words (128 bytes) using address lines A1..A6, but the IP480 uses only a portion of this space.

Refer to Table 3.1 and note that the base address for the IP module I/O space (see your carrier board instructions) must be added to the addresses shown to properly access the I/O space. Accesses are generally performed on a 16-bit basis (D0..D15), but 8-bit D08 (EO) accesses are possible in most cases.

Table 3.1: IP480 R/W Space Address (Hex) Memory Map[3]

EVEN Base Addr+	MSB D15 D08	LSB D07 D00	ODD Base Addr+
00	Counter 1 Control Register (R/W) (Not Used For 32-bit Counter)		01
02	Counter 2 Control Register (R/W) (or 32-bit Counter 1 Control Register)		03
04	Counter 3 Control Register (R/W) (Not Used For 32-bit Counter)		05
06	Counter 4 Control Register (R/W) (or 32-bit Counter 2 Control Register)		07
08	Counter 5 Control Register (R/W) (Not Used For 32-bit Counter)		09
0A	Counter 6 Control Register (R/W) (or 32-bit Counter 3 Control Register)		0B
0C	Counter 1 Read Back Register (Read Only) (or 32-bit Counter 1 Value MSW)		0D
0E	Counter 2 Read Back Register (Read Only) (or 32-bit Counter 1 Value LSW)		0F
10	Counter 3 Read Back Register (Read Only) (or 32-bit Counter 2 Value MSW)		11
12	Counter 4 Read Back Register (Read Only) (or 32-bit Counter 2 Value LSW)		13
14	Counter 5 Read Back Register (Read Only) (or 32-bit Counter 3 Value MSW)		15
16	Counter 6 Read Back Register (Read Only) (or 32-bit Counter 3 Value LSW)		17
18	Counter 1 Constant Register (Write Only)[4] (or 32-bit Counter Constant 1 MSW)		19
1A	Counter 2 Constant Register (Write Only)[4] (or 32-bit Counter Constant 1 LSW)		1B
1C	Counter 3 Constant Register (Write Only)[4] (or 32-bit Counter Constant 2 MSW)		1D
1E	Counter 4 Constant Register (Write Only)[4] (or 32-bit Counter Constant 2 LSW)		1F
20	Counter 5 Constant Register (Write Only)[4] (or 32-bit Counter Constant 3 MSW)		21
22	Counter 6 Constant Register (Write Only)[4] (or 32-bit Counter Constant 3 LSW)		23
24	Not Used[1] (Bits 15..06)	Trigger Control Register, Bits 05..00 (Write)	25
26	Not Used[1] (Bits 15..01)	Software Reset Register, Bit 00 (Write Only)	27
28	Not Used[1] (Bits 15..01)	(32-bit Counter /Timers Only) Readback Latch Control Register Bit 00 (Read/Write)	29
2A	Interrupt Pending/ Clear Register, Bits 13..08 (R/W)	Not Used[1] (Bits 07..00)	2B
2C	Not Used[1] (Bits 15..08)	Interrupt Vector Bits 07..00 (R/W)	2D
2E ↓ 7E	NOT USED[2]		2F ↓ 7F

Notes (Table 3.1):

1. These bits are not used and their state should be ignored.
2. The IP will not respond to addresses that are "Not Used".
3. Shaded register functionality only applies to IP480-6 models.
4. 8-bit accesses are possible for all registers, except the Counter Constant registers which are 16-bit access only.

This manual is presented using the “Big Endian” byte ordering format. Big Endian is the convention used in the Motorola 68000 microprocessor family and is the VMEbus convention. In Big Endian, the lower-order byte is stored at odd-byte addresses. Thus, byte accesses are done on odd address locations. The Intel x86 family of microprocessors use the opposite convention, or “Little Endian” byte ordering. Little Endian uses even-byte addresses to store the low-order byte. As such, use of this module on an ISAbus (PC/AT) carrier board will require the use of the even address locations to access the data, while a VMEbus carrier will require the use of odd address locations.

Note that for 32-bit functionality, two consecutive 16-bit registers are required. Thus, only three 32-bit counters may be configured per IP480-6 module, and one 32-bit counter per IP480-2 module. The odd-numbered 16-bit counter of the consecutive pairs always holds the Most-Significant Word (MSW) of the 32-bit value, the even-numbered counter holds the Least-Significant Word (LSW). Likewise, the corresponding even-numbered counter Control Register is used to define the 32-bit counter functionality, while the odd-numbered counter control register is ignored for 32-bit applications. In addition, the even-numbered counter input pin, clock pin, trigger pin, and interrupt pending/clear flag are used for 32-bit functionality.

REGISTER DEFINITIONS

Counter Control Registers 1-6 (Read/Write)

These registers are used to configure counter/timer functionality for the six available 16-bit timers. The lower 13-bits of these registers define the counter mode, output polarity, input polarity, external trigger polarity, trigger source, interrupt enable, counter size, clock source, internal or external counter load selection, and input debounce enable for counters 1 and 2.

Note that for 32-bit functionality, two consecutive 16-bit counters are required. Thus, only three 32-bit counters may be configured. The corresponding even-numbered counter Control Register of the odd-even pairs is used to define the 32-bit counter functionality (Counter Control registers 2, 4, & 6), while the odd-numbered counter Control Register is ignored for 32-bit applications. Likewise, the even-numbered counter inputs (trigger, clock, input) are used to control the 32-bit counter/timer.

Bits 2-0 select the counter mode. Bit 3 selects the output polarity. Bit 4 selects the input polarity. Bit 5 selects the trigger input polarity. Bit 6 selects the trigger source. Bit 7 is the Interrupt Enable bit. Bit 8 selects the counter size. Bits 9 & 10 select the clock source. Bit 11 selects internal or external counter loading for watchdog mode. Bit 12 enables debounce at the input of the counters 1 and 2 (applies to input only, not clock or trigger). Bits 15..13 are not used. Specific functionality is described in the table of the following page.

Counter Control Registers 1-6

Bit(s)	FUNCTION		
2,1,0	Specifies the Counter Mode:		
	0	000	Disabled (Default)
	1	001	Output Pulse Wave Continuous
	2	010	Output Square Wave Continuous
	3	011	Watchdog Function
	4	100	Input Pulsed Event Counter
	5	101	Input Pulse Width Measurement
	6	110	Input Period Measurement
	7	111	One-Shot Pulse Mode
3	Output Polarity (Output Pin ACTIVE Level):		
	0		Active LOW (Default)[1]
	1		Active HIGH
4	Input/Event Polarity (Input Pin Active Level):		
	0		Active LOW (Default)
	1		Active HIGH
5	External Trigger Polarity (When Bit 6 Set to 1)		
	0		High-to-LOW (Default)
	1		Low-to-HIGH
6	Trigger Source		
	0		Internal (Default)
	1		External (via Trigger input, 140ns minimum Trigger pulse required)
7	Interrupt Enable		
	0		Disable Interrupt Service (Default)
	1		Enable Interrupt Service
8	Counter Size:		
	0		16-bit Counter (Default)
	1		32-bit Counter[2]
10,9	Clock Source		
	00		Internal @ 1MHz (Default)
	01		Internal @ 4MHz
	10		Internal @ 8MHz
	11		External Clock (Up to 3.5MHz)
11	Watchdog Timer Counter Internal or External Register Load Selection:		
	0		Internal (Auto) Load of Counter
	1		Externally Triggered Load of Counter via pulse at Input pin.
12	Input Debounce Enable		
	0		Disabled - No Debounce Applied to any Input (Default)
	1		Debounce Enabled (reject Input Pulses less than or equal to 1us) for input signal of counters 1 and 2.
15,14,13[3]	Not Used[3]		

Notes (Counter Control Register):

1. The default state of the output pin is high (output has pullup installed and the drain supply jumper is present). Bit 3 specifies the active output polarity when the output is driven.
2. The counter size bit will be automatically set to 1 for the odd-numbered 16-bit counter Control Register when the 32-bit counter size has been specified in the corresponding even-numbered counter Control Register (two successive 16-bit counters implement a 32-bit counter).
3. These bits are not used and the returned state may be high or low.

Bit 11 can be used to select whether the watchdog timer counter is to be loaded from the Counter Constant Register via an external input pulse (140ns minimum pulse width), or automatically upon writing to the Counter Constant Register, in watchdog mode only.

In any mode except watchdog, when you write to the Counter Constant Register the internal counter register will be written with the same value at the same time. In watchdog mode, if bit 11 is set to 0 (default), the watchdog timer counter will be loaded internally from the Counter Constant Register, automatically upon a direct write to the Counter Constant Register. However, if bit 11 is set to 1, then the watchdog timer counter will not be loaded from the Counter Constant Register until initiated by applying a minimum 140ns pulse (polarity is programmable via bit 4) to the external counter input.

Bit 12 is used to enable the input debounce circuitry of counters 1 and 2. Debounce is applied at the counter input of counters 1 and 2 only, not the trigger or clock inputs. With input debounce enabled, input pulses less than or equal to 1us in duration will be filtered out. As such, with debounce enabled, the minimum input pulse width becomes 2us.

In watchdog timer mode, the internal watchdog counter register is loaded with the contents of the Counter Constant Register (either automatically upon writing the Counter Constant Register, or when triggered via an input pulse, as selected via bit 11 of the Counter Control Register). After triggering, the counter output goes to its active state, the output relay is energized, and this register is decremented by one each clock cycle, until it reaches 0, upon which a watchdog timer time-out occurs. At this point, the counter output returns to its inactive state, the output relay is de-energized, and an interrupt can be optionally generated. Normal (safe) operation is maintained as long as the host computer continues to cause a reload of the counter register with the contents of the Counter Constant Register before the counter reaches zero. The counter register is loaded from the Counter Constant Register via writes to the Counter Constant Register and internal auto-loading selected, or via an input pulse with external loading selected. Control of the watchdog timer output relay is summarized below:

Watchdog Timer Relay Output States

State Description	Category	Relay
MODULE NOT POWERED Host Computer Unpowered.	Unsafe	De-energized (C & B Connected)
NOT CONFIGURED Host Computer Powered, and Watchdog Timer Not Configured.	Unsafe	De-energized (C & B Connected)
TIME-OUT Host Computer Powered and Watchdog Timer Configured and has completed countdown to 0.	Unsafe	De-energized (C & B Connected)
COUNTING Host Computer Powered, Watchdog Countdown in Progress, but count has not reached 0.	Normal (Safe)	Energized (C & A Connected)

Note that the relay control follows a “failsafe” convention. That is, the relay is normally energized while counting, and then de-energized upon alarm or time-out. Note also that the counter output mirrors the action of the relay—it is driven to its active state while counting, and its inactive state upon timeout, in tandem with the relay. Optionally, an interrupt may be generated upon time-out.

Upon detection of a count value equal to 0, the watchdog timer will initiate an interrupt if enabled via bit 7 of the Counter Control Register. This could be useful for alerting the host that a watchdog timer time-out has occurred and may need to be reinitialized.

A 32-bit watchdog counter is implemented by setting bit 8 of the Counter Control Register. Three possible 32-Bit counters are formed by pairing the 16-bit counters consecutively—counters 1 & 2 form the first 32-bit counter, counters 3 & 4 the second, and counters 5 & 6 the third. The even-numbered counter of each pair is used for the counter interface and control--counters 2, 4, & 6. Counters 1, 3, & 5 are not connected and instead store the most significant two bytes of the counter value. The 32-bit count value’s least significant 16-bits are stored in the even-numbered counter’s Constant Register, while the most significant 16-bits are stored in the odd-numbered counter’s Constant Register. Likewise, the odd-numbered counter Readback Register holds the most-significant two bytes of the current count value, while the even-numbered counter Readback Register holds the least-significant two bytes of the 32-bit counter value. Both 16-bit counter outputs and one mechanical relay (relay 2, 4, & 6) are controlled in tandem by a 32-bit counter timer.

For a detailed description of the various counter modes and available control strategies, refer to the section titled “IP480 Programming”. Note that the Counter Control Register is cleared (set to 0) following a reset, thus disabling the counter/timer.

Counter Readback Registers 1-6 (Read Only)

This read-only register is a dynamic function register that returns the current value held in the counter. The contents of this register is updated with the value stored in the internal counter, each time it is read, unless the Readback Latch Control Register bit is set. The Readback Latch Control Register allows the data stored in this register upon the prior read to be frozen. This is useful for assembling a 32-bit data value with 8-bit or 16-bit accesses.

Note that for 32-bit functionality, two consecutive 16-bit registers are required. Thus, only three 32-bit counters may be configured. The odd-numbered counter of the consecutive pairs always holds the Most-Significant Word (MSW) of the 32-bit value (counters 1, 3, & 5), the even-numbered counter holds the Least-Significant Word (LSW) of the 32-bit value (counters 2, 4, & 6). Use of the Readback Latch Control Register will allow the data stored in this register upon the prior read to be frozen. This is necessary for assembling a 32-bit data value with 8-bit or 16-bit accesses.

The internal counter is generally initialized with the value in the Counter Constant Register, and its value is incremented or decremented according to the application. For event counters, this register holds the current number of events that have occurred since triggering the event counter. For input pulse-width or period measurement, this register holds the measured pulse-width or periodic rate of the input signal in number of clock cycles. In watchdog counting mode, this register holds the number of clock cycles that remain since triggering the timer and until a watchdog timer time-out will occur. For waveform generation, this register will return the current count value which can be used to determine the relative time position of the output waveform being generated. These registers are cleared (set to 0) following a system or software reset.

Counter Constant Registers 1-6 (Write Word Only)

These write-only registers are used to store the counter/timer constant values (initial value) for the various counting modes of counters 1-6. Accesses to these registers are done on a 16-bit word basis only. For event counters, this register holds the maximum count value.

For square waveform generation, this register holds the width of one pulse or half the period (in number of clock cycles). For pulse waveform generation, this register holds the periodic rate of the pulse generated (in number of clock cycles). For watchdog timers, this register stores the count-from value for the timer.

Note that in any counter mode (except when Counter Control Register bit 11 is set), when you write to the Counter Constant Register the internal counter register will be written with the same value at the same time. In watchdog mode, setting bit 11 of the Counter Control Register to 1 will instead cause the internal watchdog timer counter to be loaded from the Counter Constant Register, only after an external input pulse occurs (140ns minimum pulse width).

Note that since this register is write-only, the counter constant value cannot be read back. However, the value loaded into this register can be read back indirectly from the Counter Readback Register prior to initially counting.

For 32-bit functionality, two consecutive 16-bit registers are required, allowing only three 32-bit counters to be configured per module. The odd-numbered counter of the consecutive pairs always holds the Most-Significant Word (MSW) of the 32-bit value (counters 1, 3, & 5), the even-numbered counter holds the Least-Significant Word (LSW) of the 32-bit value (counters 2, 4, & 6).

Note that the Counter Constant Registers are cleared (set to 0) following a system or software reset.

Trigger Control Register (Write Only)

Bits 05..00 of this register are used to implement software triggering at counters 6..1, respectively. Bits 15..06 of this register are not used. When the internal trigger source has been selected for a counter function, writing a 1 to the corresponding bit position of this register will cause the counter function to be triggered. These bits are not stored and merely act as a trigger for the start of the corresponding counter function, and only when internal triggering has been enabled (internal triggering is enabled by default when bit 06 of the Counter Control Register is cleared).

Triggering may be used to initiate and re-trigger waveform generation, watchdog countdown (initiates countdown), or pulse-width or period measurement. It may also be used to initiate event counting, but unlike the other counter/timer functions, event counters will automatically recycle without re-triggering. Note that external triggering is accomplished by driving the counter trigger input to its active state.

Note that for 32-bit functionality, two consecutive 16-bit registers are required. Thus, only three 32-bit counters may be configured. The Trigger Control Register bits corresponding to the even-numbered counters are used to trigger 32-bit counter/timer functions (counters 2, 4, & 6).

Software Reset Register (Write Only)

Writing a 1 to the bit 00 position of this register will cause a software reset to occur. This bit is not stored and merely acts as a trigger for software reset generation (this bit will always readback as 1). The effect of a software reset is similar to a carrier reset, except that it is not driven by the carrier and it does not reset the Interrupt Vector. That is, bits 07..00 of the Interrupt Vector Register are not cleared in response to a software reset. This control is useful for use with some ISA carriers which do not implement the bus reset control. Bits 15..01 of this register are not used and will always read high (1's).

Readback Latch Control Register (Read/Write)
For 32-bit Counter/Timer Functions Only

Because this module may be used to implement 32-bit register functions, while only supporting 8 and 16-bit data accesses, setting bit 00 of this register will cause the last data loaded into the Counter Readback Registers to be frozen, thus enabling the entire 32-bit counter value to be assembled using multiple 8-bit or 16-bit read cycle accesses. That is, for 32-bit counter functions, it takes two read cycles to access the data with 16-bit accesses—one read cycle executed on the MSW (Most Significant Word), one on the LSW (Least Significant Word). In 32-bit mode, any read cycle executed on either the 16-bit LSW or MSW register will cause the latest 32-bit counter value to be simultaneously loaded into both registers while bit 00 is clear. Then, if bit 00 of the Readback Latch Control Register is set, the current register data just latched into both registers cannot be over-written. Thus, setting this bit after the first 16-bit read allows the entire 32-bit value to be latched without causing a new data value to be loaded upon the next read. Because, whenever the Readback Registers are read with bit 00 clear (0), they are updated with the current (latest) data from their corresponding counter. Setting this bit prevents you from assembling an erroneous count value due to a change in counter value between the first and second read cycles. Typically, bit 00 of this register is set after the first 8 or 16-bit read cycle to inhibit latching a new value into the Readback Registers upon the second read cycle, thus enabling the previously latched 32-bit value to be read using 16-bit or 8-bit accesses.

It is important to remember that the Counter Readback Registers are loaded with a new (current) value upon reading the register with the Readback Latch Control bit cleared. If the Readback Latch Control bit is set before reading either of the two 16-bit registers that make up the 32-bit counter value, then the current read will actually be read an old value--a value that was latched into the registers upon some read cycle prior to setting the Readback Latch Control Register bit. This is why it is necessary to set this bit after the first read cycle and before the second—the first read cycle latches the current data, then setting this bit freezes the register contents, and the second read cycle retrieves the frozen data. This bit would then have to be cleared to allow further updates to the Counter Readback Registers.

Bit 00 of this register is cleared following a reset. Bits 15..01 of this register are not used and should be ignored.

Interrupt Pending/Clear Register (Read/Write)

Bits 13..08 of this register are used to flag (read) and clear (write) pending interrupts at counters 6..1, respectively. When read, a set bit (1) indicates that the corresponding counter has an interrupt pending. Writing a "0" to this bit will clear the interrupt pending at the corresponding counter channel. For two counter Model IP480-2 units, only bits 08 & 09 of this register are used for counter 1 and counter 2, respectively.

Interrupt Pending/Clear Register

BITS	FUNCTION
13..08	Counter 6..1 Interrupt Pending Flag (Read) Counter 6..1 Interrupt Clear Bit (Write "0")
15..10	(IP480-2) Not Used
15, 14	(IP480-6) Not Used

Interrupts may be generated for several different conditions. Interrupt enable bit 07 of the Counter Control Register is used to enable interrupts for a counter channel. Interrupts may be generated when an event count reaches the value stored in the Counter Constant Register. They may also be generated when a pulse-width or periodic-rate measurement has been completed. A watchdog timer time-out can also generate an interrupt. Likewise, an interrupt may be triggered when a pulse waveform has been completed (one-shot pulse mode), or each time a successive waveform is generated (continuous mode). Similarly, in continuous square wave mode, an interrupt may be generated upon each transition of the square wave output (rising or falling) when enabled.

Bits 13..08 are cleared following a system or software reset. Bits 14 & 15 of this register are not used and should be ignored. For IP480-2 models, bits 15..10 of this register are not used and should be ignored.

Interrupt Vector Register (Read/Write)

This 8-bit read/write register is used to store the interrupt vector. In response to an interrupt select cycle, the IP module will execute a read of this register. This register is cleared following a system reset, but not a software reset.

IP Identification Space - (Read Only, 32 Odd-Byte Addresses)

Each IP module contains identification information that resides in the ID space per the IP module specification. This area of memory contains 32 bytes of information at most. Both fixed and variable information may be present within the ID space. Fixed information includes the "IPAC" identifier, model number, and manufacturer's identification codes. Variable information includes unique information required for the module. The IP480 ID information does not contain any variable (e.g. unique calibration) data. ID space bytes are addressed using only the odd addresses in a 64 byte block on the "Big Endian" VMEbus. Even addresses are used on the "Little Endian" PC bus. The IP480-X ID space contents are shown in Table 3.2. Note that the base-address for the IP module ID space (see your carrier board instructions) must be added to the addresses shown to properly access the ID space.

Table 3.2: IP480-X ID Space Identification Contents

Hex Offset From ID Space Base Address	ASCII Character Equivalent	Numeric Value (Hex)	Field Description
01	I	49	All IP's have 'IPAC'
03	P	50	
05	A	41	
07	C	43	
09		A3	Acromag ID Code
0B		16	IP480-6 Code[1]
		17	IP480-2 Code[1]
0D		00	Not Used (Revision)
0F		00	Reserved
11		00	Not Used (Driver ID Low Byte)
13		00	Not Used (Driver ID High Byte)
15		0C	Total Number of ID Space Bytes
17		1E	IP480-6 CRC
		7F	IP480-2 CRC
19 to 3F		yy	Not Used

Notes (Table 3.2):

1. The IP model number is represented by a two-digit code within the ID space (the IP480-6 model is represented by 16 Hex, the IP480-2 model is represented by 17 Hex).
2. Execution of an ID space read requires 0 wait states.

THE EFFECT OF RESET

A power-up or bus-initiated reset will place the module in the default state and disable the counter/timers. It will stop and clear the counter and any interrupts, and reset the timers. A reset will also clear all I/O registers and set the counter open-drain output pin to the high (default) state.

Another form of reset initiated via the Software Reset Register acts similar to a carrier or power-up reset, except that it is not driven by the carrier and will preserve the contents of the Interrupt Vector Register (writing a 1 to the bit 0 position of the Software Reset Register will cause this type of reset to occur). Resets in this manner have been provided for use with some ISA carriers which do not implement the bus reset control, or when the interrupt vector information must be preserved following reset.

IP480 PROGRAMMING

Acromag provides an Industrial I/O Pack Software Library diskette (Model IPSW-LIB-M03, MSDOS format) to simplify communication with the board. Example software functions are provided for both ISAbus (PC/AT) and VMEbus applications. All functions are written in the "C" programming language and can be linked to your application. For more details, refer to the "README.TXT" file in the root directory on the diskette and the "INFO480.TXT" file in the appropriate "IP480" subdirectory off of "\VMEIP" or "\PCIP", according to your carrier.

Acromag also provides a software diskette of Industrial I/O Pack Object Linking and Embedding (OLE) drivers for Windows 95 and Windows NT compatible application programs (Model IPSW-DVR-OLE-PC, MSDOS format).

This software provides individual drivers that allow Acromag I/O Packs and the APC8610 carrier to be easily integrated into Windows application programs, such as Visual C++, Visual Basic, etc. The OLE controls provide a high-level interface to Acromag I/O Packs, eliminating the need to perform low-level reads/writes of registers, and the writing of interrupt handlers—all the complicated details of programming are handled by the OLE controls. These functions are intended for use in conjunction with the Acromag APC8610 ISAbus (PC/AT) carrier and consist of a Carrier Configuration Program, and APC8610 OLE control, and an OLE control for each Acromag I/O Pack model.

The following sections describe various C/T functions and control operation.

Pulse & Square Waveform Generation (Counter Modes 1 & 2)

Pulse & square waveforms may be generated at the timer output pins. Square waveforms are generated continuously. Pulse waveforms may be generated continuously, or for one cycle (one-shot mode). Waveform generation is configured via bits 0-3 of the Counter Control Register. Internal or external clocking and triggering are possible. Optionally, an interrupt may be generated when a pulse waveform has been completed (one-shot mode), or upon generation of each successive waveform following the first (continuous mode).

A continuous square wave may be generated at the counter output pin in counter mode 2. Square waves are generated continuously once triggered. The output square wave has a duty cycle (half the period) that is specified by the value written to the Counter Constant Register. The counter goes through two full countdown sequences for each cycle. When the 1 count is detected, on the next rising-edge of the clock, the output toggles to the opposite state and the Counter Constant Register value is reloaded into the counter register, and countdown resumes, decrementing by one each clock cycle. As such, with an internal clock frequency of 8MHz, a square wave with a maximum frequency of 4MHz is possible (maximum frequency is half the clock frequency). Due to the method employed in synching an external clock to the internal IP clock, a waveform period may vary ± 125ns from what is expected if the counter/timer is clocked externally. Waveform generation may be triggered externally via the Trigger input, or internally via the Trigger Control Register, according to the state of the trigger source bit 6 in the Counter Control Register. An initial trigger, software or external, causes the count-down sequence to begin and a continuous square waveform to be generated (no re-trigger required).

In counter mode 1, pulse mode waveforms provide an output pulse that is asserted for one clock cycle, beginning when the internal down-counter leaves a count of 1. When the 1 count is detected, on the rising-edge of the clock, the output will toggle to the opposite state and the counter constant value will be reloaded into the counter register, and countdown will resume. Thus, the period is determined by the value written to the Counter Constant Register. In counter mode 7 (one-shot pulse mode), a pulse waveform will be generated one time and repeated only each time it is re-triggered. Note that a pulse waveform can be generated continuously in counter mode 1. Upon pulse waveform completion (one-shot mode), or upon generation of each successive waveform (continuous mode), an optional interrupt can be generated if the interrupt enable bit 7 of the Counter Control Register is set.

Varying the clock rate controls the pulse-width (i.e. 125ns @ 8MHz, 250ns @ 4MHz, 1us @ 1MHz, etc). Due to the method employed in synching an external clock to the internal IP clock, a waveform period may vary ± 125ns from what is expected if the counter/timer is clocked externally. The triggering and clocking operation are the same as described for the square wave above.

Note that for continuous square or pulse waveform generation, an interrupt may be generated (if enabled) upon the rising or falling edge of each new square-wave, or upon start of each new pulse waveform. In one-shot mode, an interrupt may be generated when the single pulse waveform has been completed.

Note that for 32-bit counter functionality, two consecutive 16-bit registers are required. Thus, only three 32-bit counters may be configured per IP480-6 module (one for IP480-2 units). The odd-numbered counter of the consecutive pairs always holds the Most-Significant Word (MSW) of the 32-bit value (counters 1, 3, & 5), the even-numbered counter holds the Least-Significant Word (LSW) of the 32-bit value (counters 2, 4, & 6). In 32-bit mode, a waveform is generated at both the odd and even-numbered counter outputs, but configured only through the even-numbered counter's Control Register.

Watchdog Timer Operation (Counter Mode 3)

The watchdog timer will countdown from a programmed value until it reaches 0 and a time-out is generated. While counting, the counter output will mirror the operation of the relay—the output will go to its active state while the relay is energized. Upon time-out, the counter output will return to its inactive state, the corresponding mechanical relay will be de-energized, and an optional interrupt may be generated. If a 32-bit watchdog timer is implemented, then both 16-bit counter outputs and relays are controlled in tandem. Following the "failsafe" convention, the output relay is only energized while the watchdog timer is counting. A watchdog timer that has timed-out will not re-cycle until it is re-triggered following a load of the counter/timer register. The counter/timer register can only be loaded two ways: by writing to the Counter Constant Register with auto-loading enabled (Counter Control Register bit 11=0), or by generating an input pulse (140ns minimum) at the input pin with auto-loading inhibited (Counter Control Register bit 11=1). Failure to cause a reload of the internal counter/timer register would generate an automatic time-out upon re-triggering, since the counter register still contains the 0 it has counted down to.

The Counter Constant Register holds the count-from value for the timer. The internal counter/timer register is loaded with the contents of the Counter Constant Register either automatically upon writing the Counter Constant Register, or when triggered via an input pulse, as selected via bit 11 of the Counter Control Register.

The watchdog timer may be triggered internally (via the Trigger Control Register), or externally (via the Trigger input signal). When triggered, the counter/timer register contents is decremented by one each clock cycle, until it reaches 0, upon which a watchdog timer time-out occurs. The current contents of the counter/timer register can be read from the Counter Readback Register. The timer may be clocked via the internal 1MHz, 4MHz, or 8MHz clock, or by an external clock up to 3.5MHz at the counter clock pin. Due to the asynchronous relationship between the trigger and the selected clock, the time-out may occur ± 125ns from the selected clock period. Upon time-out, the counter output pin returns to its inactive state and an interrupt can be optionally generated.

Additionally, the watchdog timer also controls the state of an isolated electro-mechanical SPDT relay. Control of this relay via the watchdog timer is summarized in the following table:

Watchdog Timer Relay Control

State Description	Category	Relay
NOT POWERED Host Computer Unpowered.	Unsafe	De-energized (C & B Connected)
NOT CONFIGURED Host Computer Powered, and Watchdog Timer is Not Configured.	Unsafe	De-energized (C & B Connected)
TIME-OUT Host Computer Powered and Watchdog Timer is Configured and has completed countdown to 0.	Unsafe	De-energized (C & B Connected) AND Counter Output Returns to Inactive State
COUNTING Host Computer Powered, Watchdog Countdown in Progress, but count has not reached 0.	Normal (Safe)	Energized (C & A Connected) AND Counter Output Sent to Active State

Note that the relay control follows a “failsafe” convention. That is, the relay is normally energized, and then de-energized upon alarm or time-out. Note also that the counter output mirrors the action of the relay in watchdog timer mode (the output polarity is programmable).

Note that normal (safe) operation is maintained as long as the host computer continues to cause a reload of the counter register with the contents of the Counter Constant Register before the counter reaches zero and a time-out occurs (via writes to the Counter Constant Register and internal auto-loading, or by providing an external input pulse with auto-loading inhibited). After a time-out has occurred, the normal (safe) state will not reoccur until the counter/timer is re-triggered after causing a reload of its register.

Upon detection of a count value equal to 0, the IP480 will issue an interrupt if enabled via bit 07 of the Counter Control Register. This could be useful for alerting the host that a watchdog timer time-out has occurred and may need to be reinitialized.

A 32-bit watchdog counter is implemented by setting bit 8 of the Counter Control Register. Three possible 32-Bit counters are formed by pairing the 16-bit counters consecutively—counters 1 & 2 form the first 32-bit counter, counters 3 & 4 the second, and counters 5 & 6 the third. The even-numbered counter of each pair is used for the 32-bit counter interface and control--counters 2, 4, & 6. Counters 1, 3, and 5 are not connected and instead store the most significant two bytes of the count value. The 32-bit count-from value’s least significant 16-bits are stored at the even-numbered counter’s Constant Register, while the most significant 16-bits are stored at the odd-numbered counter’s Constant Register. Likewise, the even-numbered counter’s Readback Register reflects the least significant two bytes of the current count value, while the odd-numbered counter’s Readback Register reflects the most-significant two bytes of the 32-bit counter value. Use of the Readback Latch Control Register will allow the data that was stored in the Counter Readback Register during the prior read to be frozen. This is necessary for assembling a 32-bit readback value with 8-bit or 16-bit accesses.

Note that in 32-bit mode, both counter outputs and mechanical relays are controlled in tandem. In addition, the counter size bit 8 of the odd-numbered 16-bit counter‘s Counter Control Register will be automatically set to indicate 32-bit mode upon configuring the corresponding even-numbered counter for 32-bit mode.

Event Counting (Counter Mode 4)

Bits 02..00 of the Counter Control Register are used to configure a channel for event counting by selecting counter mode 4. Positive or negative events may be tallied, as selected via the input polarity bit of the Counter Control Register (bit 04). In this mode, input pulses or events occurring at the input pin of each counter channel may be counted up to a programmed count limit. Upon reaching the count limit, the counter output will generate a 1us pulse, an optional interrupt can be generated, and the internal event counter register is then cleared. Once triggered, an event counter will continuously wrap around to its count limit to prevent lost events—no re-triggering is required.

The Counter Constant Register holds the count-to value (constant), reading the Counter Readback Register will return the current count (variable). In event counter mode, the input event serves as an enable to count an event. A minimum event pulse width of 140ns is required for correct pulse detection with input debounce disabled. With debounce enabled at counters 1 and 2, a minimum event pulse width of 2us is required for correct detection. Internal or external clock selection has no effect for event counters. Event counting may be initially triggered internally (via the Trigger Control Register), or externally (via the Trigger input signal). To prevent missing events, the counter will continuously wrap around and resume counting up from zero, without requiring a new trigger each time the count limit is reached. Upon reaching the count limit, a 1us pulse will be generated at the counter output pin, and an optional interrupt may be generated.

If the Interrupt Enable bit of the Counter Control Register is set (bit 07), an interrupt is generated when the number of input pulse events is equal to the constant value stored in the Counter Constant Register. The internal counter register is then cleared and will continue counting events until the counter constant value is again reached and a new interrupt generated. The Interrupt Pending/Clear register can be read to determine which counter(s) generated the interrupt. Note that the IP480 will continue to interrupt and reinitialize itself in event counting mode without operator intervention. The trigger (internal or external) is only required initially to start the cycle.

A 32-bit event counter is accomplished by setting bit 08 of the Counter Control Register. Three possible 32-Bit counters are formed by pairing the counters consecutively—counters 1 & 2 form the first 32-bit counter, counters 3 & 4 the second, and counters 5 & 6 the third. The even-numbered counter of each consecutive pair is used for the 32-bit event counter configuration and control--counters 2, 4, and 6. Counters 1, 3, and 5 are not used and instead store the most significant two bytes of the 32-bit count value.

The 32-bit count value’s least significant 16-bits are read from the even-numbered counter’s Constant Register & Counter Readback Register, while the most significant 16-bits are read from the odd-numbered counter’s Constant Register & Counter Readback Register. Use of the Readback Latch Control Register will allow the data that was stored in the Counter Readback Register during the prior read to be frozen.

This is necessary for assembling the 32-bit data value with 8-bit or 16-bit accesses. The even-numbered counter's input, clock, and trigger pins are used to control the 32-bit counter, while the odd-numbered counter's input pins are ignored.
In addition, the interrupt pending/clear flag of the even-numbered 16-bit counter channel is used for the 32-bit counter, while the odd-numbered interrupt pending/clear flag is ignored. However, 32-bit counters will generate a 1us pulse at both 16-bit counter outputs upon reaching the 32-bit count limit.

Input Pulse Width Measurement (Counter Mode 5)

The IP480 may also be used to accomplish input pulse-width measurement for pulses occurring at the counter input pin. Pulse-width measurement may be triggered internally via the corresponding Trigger Control Register, or externally via the counter Trigger input signal. Bits 2..0 of the Counter Control Register are used to configure the channel for pulse-width measurement. An internal 1MHz, 4MHz, or 8MHz clock, or an external clock (up to 3.5MHz) is used to set the measurement resolution by acting as an enable for the counter which is internally clocked at 8MHz. The polarity of the pulse is configured via input polarity bit 4 of the Counter Control Register.

For pulse-width measurement, the pulse-width being measured serves as an enable control for an up-counter whose value can be read from the Counter Readback Register. When triggered, the counter increments by one for each clock pulse while the input signal level remains in the active state (high or low according to the programmed polarity). The up-counter may use an internal clock, or an external clock at the counter's clock pin (up to 3.5MHz). As such, the resultant measurement will have a resolution of the inverse of the clock frequency. The resultant pulse-width is equivalent to the count value read from the Counter Readback Register, multiplied by the clock rate. A 1us pulse will be generated at the counter output pin to signal the completion of a given measurement. Optionally, upon completion of a given pulse width measurement (the pulse has returned to the opposite polarity), the IP module will issue an interrupt if enabled via the interrupt enable bit of the Counter Control Register (bit 07). Note that the measured pulse width may be in error by $\pm$ 1 clock cycle.

A 32-bit pulse width measurement is accomplished by setting bit 8 of the Counter Control Register. In this mode, up to three possible 32-Bit counters may be formed by pairing the 16-bit counters consecutively—counters 1 & 2 form the first 32-bit counter, counters 3 & 4 the second, and counters 5 & 6 the third. The even-numbered counter of each consecutive pair is used for the pulse interface and configuration--counter 2, 4, & 6. Counters 1, 3, & 5 are not connected and instead store the most significant two bytes of the pulse-width value in the corresponding Counter Readback Register. Use of the Readback Latch Control Register will allow the data stored in these registers upon the prior read to be frozen. This may prove useful in assembling a 32-bit data value with 8-bit or 16-bit accesses, when the counter value continues to change.

Input Period Measurement (Counter Mode 6)

The IP480 may be used to measure the period of an input signal at the counter input pin. Bits 02..00 of the Counter Control Register are used to configure the channel for periodic-rate measurement. Period measurement is accomplished the same way as described above for pulse-width measurement, except that the Counter Readback Register holds the period of the input signal (in number of clock cycles), not just the width of the high or low pulse. Note that the measured period may be in error by $\pm$ 1 clock cycle.

Interrupt Generation

Interrupts may be generated for several different conditions. Interrupt enable bit 07 of the Counter Control Register is used to enable interrupts for a counter channel. Interrupts may be generated when an event count reaches the value stored in the Counter Constant Register. They may also be generated when a pulse-width or periodic-rate measurement has been completed. A watchdog timer time-out can also generate an interrupt. Likewise, when a pulse waveform has been completed (one-shot mode), an interrupt may be triggered. Continuous waveforms may also generate interrupts upon the start of each new pulse, or upon the rising or falling edge of each square wave cycle.

After pulling the IntReq0 line low and in response to an Interrupt Select cycle, the module will read (serve) the 8-bit interrupt vector stored in the Interrupt Vector Register. The IntReq0 line will be released as soon as the conditions generating the interrupt have been cleared or return to normal, a reset occurs, or until the Interrupt Pending/Clear bit of the Interrupt Vector Register is cleared. Zero wait states are required to complete an interrupt select cycle.

Programming Examples

Event Counter

The following example outlines the basic steps necessary to configure the IP480 as an event counter. In this example, the event counter is input to counter channel 1 and is to count to 1000 (03E8 Hex), then generate an interrupt. The event counter is to be triggered internally and is to count positive events (event counters do not use a clock signal). It is assumed that the IP480 module has already been reset and no prior (non-default) configuration exists.

1. After reset, the counter/ timers are initially disabled (counter mode 0). Begin programming by writing 03E8H to the Counter 1 Constant Register. This is equivalent to 1000 and is the value that the event counter is to count to before generating an interrupt.
2. Write an 8-bit interrupt vector to the Interrupt Vector Register. This is the value that will be read in response to an interrupt select cycle after generating an interrupt.
3. Next write to the Counter Control Register to configure the counter. The breakdown of this register content is as follows:

    - Event counting is counter mode 4. Thus, bits 02..00 are to be set to "100".
    - An active high output polarity is desired, so set bit 03 to "1".
    - Positive events are to be counted, so set the input polarity bit 04 to "1".
    - Since no external triggering is used, bit 05 should be "0".

- Since internal triggering is used, set trigger source bit 06 to "0".
- Since an interrupt is to be generated upon 0 count, set bit 07 to "1" to enable interrupts.
- Since a count of 1000 will fit into a 16-bit value, set the counter-size bit 08 to "0" for 16-bit counter size.
- Since event counters do not use the clock input, set bits 10..09 to "00", respectively.
- Bit 11 is not used for event counters so set this bit to "0".
- Bit 12 is set to "0" to disable input debounce.
- Bits 15..13 are not used so set these bits to "000".

Thus, the 16-bit result is "0000 0000 1001 1100" or 009CH. Write "009CH" to the Counter 1 Control Register. The counter is now awaiting a trigger to initiate event counting.

4. Trigger the event counter internally by writing "0001H" to the Trigger Control Register.
5. Since an 8MHz internal clock is used, a positive event pulse must go active for at least 140ns to be recognized as a valid event. Begin generating events at the counter 1 input pin.
6. Read the current count value by reading the counter 1 Readback Register.
7. After 1000 events have occurred, a 1us pulse will be generated at the counter 1 output pin and an interrupt will be generated (IntReq0 line taken low). An interrupt select cycle should be performed and the IP480 will serve up its 8-bit interrupt vector.
8. At this point, the Interrupt Pending/Clear Register can be read to determine which counter generated the interrupt. For our example, bit 00 should indicate a "1" since counter 1 generated the interrupt.
9. Write "00H" to the Interrupt Pending/Clear Register to clear the interrupt generated by counter 1.
10. As events continue to occur, the IP480 event counter will continue to count to 1000, generate another interrupt, and recycle as described above, until a reset occurs or the counter mode is changed.

Watchdog Timer

The following example outlines the basic steps necessary to configure the IP480 watchdog timer function. In this example, a 16-bit timer is implemented at channel 1 counting down from 65535 (FFFF Hex). Upon zero count, a time-out interrupt will be generated. The timer counter is to auto-load, be triggered internally, and clocked internally at 1MHz. It is assumed that the IP480 module has already been reset and no prior (non-default) configuration exists.

1. After reset, the counter/ timers are initially disabled (counter mode 0). Begin programming by writing FFFFH to the counter 1 Constant Register. This is equivalent to 65535 decimal and is the value that the timer is to begin counting from before generating a time-out interrupt upon reaching zero.

2. Write an 8-bit interrupt vector to the Interrupt Vector Register. This is the value that will be read in response to an interrupt select cycle after generating an interrupt.

3. Next write to the counter 1 Control Register to configure the counter. The breakdown of this register content is as follows:

   - The watchdog function is counter mode 3. Thus, bits 02..00 are to be set to "011".
   - An active high output polarity is desired, so set bit 03 to "1".
   - The input is not used, so set the input polarity bit 04 to "0".
   - Since no external triggering is used, external trigger polarity bit 05 should be "0".
   - Since internal triggering is used, set trigger source bit 06 to "0".
   - Since an interrupt is to be generated upon 0 count, set bit 07 to "1" to enable interrupts.
   - Since a count of 65535 will fit into a 16-bit value, set the counter-size bit 08 to "0" for 16-bit counter size.
   - Since the counter is to be clocked internally at 1MHz, set bits 10..09 to "00", respectively.
   - Since internal (automatic) loading of the watchdog timer counter is desired, set bit 11 to "0".
   - Bit 12 is set to "0" since input debounce is not used.
   - Bits 15..13 are not used so set these bits to "0000".

   Thus, the 16-bit result is "0000 0000 1000 1011" or 008BH. Write "008BH" to the Counter 1 Control Register. The watchdog timer is now awaiting a trigger to initiate countdown.

4. Trigger the counter internally by writing "0001H" to the Trigger Control Register.

   Since a 1MHz internal clock is used, every clock cycle (1us) the timer count value is decremented by 1.

5. Read the current count value by reading the counter 1 Readback Register. This value is the number of clock cycles remaining till time-out.

   Normal (safe) operation is maintained as long as the host computer continues to cause a reload of the counter register before the counter reaches zero (via writes to the Counter Constant Register which will auto-load the counter). Reloading the counter register after the counter reaches 0 would require that the watchdog timer be re-triggered to re-cycle.

7. After 65535 clock cycles have occurred (65535us), the counter 1 output pin will go to its inactive state and an interrupt will be generated (IntReq0 line taken low). Note that the output pin is driven active while the relay is energized. An interrupt select cycle should be performed and the IP480 will serve up its 8-bit interrupt vector.

   Note that a slower external clock might make this timer more useful as it would increase the time until time-out, and/or a 32-bit timer may be configured allowing larger count values.

8. At this point, the Interrupt Pending/Clear Register can be read to determine which counter generated the interrupt. For our example, bit 08 should indicate a "1" since counter 1 generated the interrupt.

9. Write "00H" to the Interrupt Pending/Clear Register to clear the interrupt generated by counter 1.

10. Upon reaching a count of 0, the IP480 watchdog timer will require another trigger to recycle as described above.

4.0 THEORY OF OPERATION

This section provides a description of the basic functionality of the circuitry used on the board. Refer to the Drawing 4501-609 as you review this material.

IP480 OPERATION

The IP480 uses an FPGA (Field Programmable Gate Array) to provide its I/O interface and configuration functionality. Six different counter/timer modes may be selected.

Field inputs to the FPGA are buffered using octal-buffered line drivers. Field inputs to these buffers include transient protection devices on each line and 4.7K pullups to +5V.

Counter outputs are the open drains of n-channel mosfets. Drains are pulled-up to +5V on board (default), or to the external supply pin (according to the placement of the supply jumper) using a socketed resistor SIP (470Ω and 4.7KΩ SIP's are provided). The SIP may be easily removed or replaced for convenient drive level adjustment. Likewise, the use of an external supply allows the drain pullups to adjust to different drive levels. Outputs include transient protection devices on each line.

The IP480 also includes electromechanical SPDT (1 Form C) relays which work in tandem with the counter outputs, but are only triggered via watchdog timer time-out. These relays are normally energized while the watchdog timer is counting, then de-energized upon reaching a count of 0 (time-out), for true "failsafe" operation.

The FPGA installed on board provides the control interface necessary to operate the module, plus the IP identification memory required per the IP specification.

LOGIC/POWER INTERFACE

The logic interface to the carrier board is made through connector P1 (refer to Table 2.2). P1 also provides +5V to power the module (the ±12V lines are not used). Not all of the IP logic P1 pin functions are used.

The FPGA installed on the IP Module provides the control signals required to operate the board. It decodes the selected addresses in the I/O, Interrupt, and ID spaces and produces the chip selects, control signals, and timing required by the control registers, as well as, the acknowledgment signal required by the carrier board per the IP specification. It also stores the interrupt vector.

The ID space (read only) is also implemented in the FPGA and provides the identification for the individual module per the IP specification. The ID space and the configuration and control registers are all accessed through a 16-bit data bus interface to the carrier board.

5.0 SERVICE AND REPAIR

SERVICE AND REPAIR ASSISTANCE

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be easily damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board. When a board is first produced and when any repair is made, it is tested, placed in a burn-in room at elevated temperature, and retested before shipment.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

PRELIMINARY SERVICE PROCEDURE

Before beginning repair, be sure that all of the procedures in Section 2, Preparation For Use, have been followed. Also, refer to the documentation of your carrier board to verify that it is correctly configured. Replacement of the module with one that is known to work correctly is a good technique to isolate a faulty module.

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

Acromag's Application Engineers can provide further technical assistance if required. When needed, complete repair services are also available from Acromag.

6.0 SPECIFICATIONS

GENERAL SPECIFICATIONS

Operating Temperature.....Standard units are 0 to +70°C. "E" suffixed units are -40°C to +85°C.
Relative Humidity.....5-95% non-condensing.
Storage Temperature.....-55°C to +125°C.
Physical Configuration.....Single Industrial I/O Pack Module.
- Length.....3.880 inches (98.5mm).
- Width.....1.780 inches (45.2mm).
- Board Thickness.....0.062 inches (1.59mm).
- Max Component Height.....Less than 0.314 inches (7.97mm).

Connectors:
- P1 & P2 .....IP logic (P1) & field (P2) interface connectors - 50-pin female receptacle header (AMP 173279-3 or equivalent).

Power:
- +5 Volts (±5%).....IP480-6/6E 190mA, Typical; 255mA, Maximum. IP480-2/2E 95mA, Typical; 110mA, Maximum. Note: At power up the +5V supply must rise from 3V to 4.75V in less than 4ms to guarantee proper configuration of the module's FPGA.
- ±12 Volts (±5%) from P1.....0mA Maximum (Not Used).

Isolation.....The watchdog timer's electro-mechanical relay contacts are isolated for voltages up to 125VAC @1A, continuous (unit will withstand a 1250VAC dielectric strength test for one minute without breakdown). This complies with test requirements outlined in ANSI/ISA-S82.01-1988 for the voltage rating specified. Note that all counter I/O lines share a common connection.

Resistance to RFI.....Designed to comply with IEC1000-4-3 Level 3 (10V/m, 27 to 500MHz) and European Standard EN50082-1 with no data upsets.

Resistance to EMI.....Unit has been tested and no data upsets occur under the influence of EMI from switching solenoids, commutator motors, and drill motors.

ESD Protection..... Complies with IEC1000-4-2 Level 1 (2KV direct contact discharge at input/output terminals) and European Standard EN50082-1.

Surge Withstand Capability.....Inputs/outputs exhibit no damage when tested with a standardized 2.5KV test waveform represent-ative of surges (high frequency transient electrical interference) per ANSI/IEEE C37.90-1978.

EFT Protection……Complies with IEC1000-4-4 Level 2 (0.5KV at input and output terminals) and European Standard EN50082-1.

Radiated Emissions……Designed to comply with European Standard EN55022 for class B equipment with a shielded enclosure port.

COUNTER/TIMERS

Configuration……..IP480-6/IP480-6E: six 16-bit or three 32-bit counter/timer functional groups. IP480-2/IP480-2E: two 16-bit or one 32-bit counter/timer functional groups. Each counter/timer consists of a clock input, an event/signal input, a trigger input, an open-drain output, and a SPDT mechanical relay output. Transient Voltage Suppression (TVS) devices are installed at each I/O line for transient & over-voltage protection. Two 16-bit counter timers are used to implement 32-bit counter/ timer functionality.

Counter Modes……..Seven functional modes including event counter, pulse or square wave generator, pulse-width monitor, waveform period monitor, and watchdog timer.

Speed…….. Maximum output pulse or square wave frequency: 4MHz; Minimum event pulse width 140ns (debounce disabled), 2us (debounce enabled); Minimum pulse width measurement: 250ns (debounce disabled), 2us (debounce enabled); Minimum period measurement: 500ns (debounce disabled), 2us (debounce enabled). Rate will vary with clock frequency (use of the 8MHz internal clock is assumed here). Output speed will also vary with output pullup SIP installed (see Output Open-Drain Pullups).

Mode Accuracy…..Waveform Generation: period is ±125ns with external clocking; Watchdog Function: time-out occurs within ±1 clock cycle with external clocking; Pulse/Period Measurement: ±1 clock cycle.

Clocking……..Programmable internal or external. Clocks are not used for event counters.

Internal Clocks……Programmable 1MHz, 4MHz, or 8MHz via the Counter Control Register.

External Clocks……..Separate clock input for each counter supports frequencies up to 3.5MHz.

Debounce (Counter 1-2 Input)..No debounce (default). Input debounce enabled via bit 12 of Counter Control Register. Applies to Counters 1 and 2 only. Debounce will filter out all input pulses less than 1us in duration. The minimum acceptable input pulse width is 2us with debounce enabled.

Interrupts.....Interrupts can be generated for several different conditions: watchdog timer time-out, event count complete, pulse-width or periodic rate measurement complete, pulse wave complete (one-shot mode), and successive waveform generation (continuous).

Triggering……Programmable internal via register write, or external via trigger input with programmable polarity. Internal triggering is accomplished via a register write to the Trigger Control Register. External triggering is done via the counter/ timer trigger input. Internal or external triggering is selected via bit 6 of the Counter Control Register. A minimum low or high pulse width of 140ns is required.

Counter Trigger……..External trigger inputs for triggering counter functions. Input level is TTL or CMOS compatible with V_{IH}=2.0V and V_{IL}=0.8V. Inputs are buffered and include 4.7K pullups to +5V.

Counter Input…..……Interface for events, and pulse & period measurements. May also be used to trigger load of watchdog timer register. Input level is TTL or CMOS compatible with V_{IH}=2.0V and V_{IL}=0.8V. Inputs are buffered and include 4.7K pullups to +5V. Optional debounce may be selected for counters 1& 2 input only via bit 12 of the Counter Control Register.

Input Requirements……Input voltage range is -0.25V to 5.25V. Logic inputs have 2.0V DC Minimum High Level; 0.8V DC Maximum Low Level; 10uA Maximum current.

Input Hysteresis……..200mV typical.

Counter Output……Non-Isolated open-drains of N-channel mosfets with socket for pullup resistor SIP installation. SIP common may be pulled up to +5V on board, or to the P2 external supply pin for convenient level and/or response time adjustment. Output drains are protected to 60V DC and may sink up to 250mA each. Outputs are driven to their active level during watchdog time-out. They generate a 1us pulse upon pulse-width or period measurement complete, event-count reached, and are cycled during waveform generation.

Output Voltage Range……Outputs are low-side switches and are rated for 0-5V with pullups strapped to internal supply (default position); or 0-60V with pullups to an external 0-60V supply. Note that pullup values must be increased for external supplies greater than 26V (4.7KΩ), or 8V (470Ω), to limit SIP resistor power dissipation to less than 0.15W per resistor.

Output Open-Drain Pullups……Resistor SIP (R2) is installed in socket X1 (refer to Drawing 4501-610). A 4.7KΩ & 470Ω SIP is provided and packaged separately. Power is limited to 0.15W per resistor. This value may be easily removed or replaced to adjust the output drive capability or affect response time. For example: with the 4.7KΩ SIP installed, the outputs will reach 90% of their final level in 10us typical. Use of the 470Ω SIP reduces this time to 1us typical. Do not exceed the rated power capability of this resistor or damage may result. This SIP can be pulled up to the +5V board supply (default), or to the external supply pin, according to the supply jumper position (see Drawing 4501-610).

Output Relays……Two (“-2” units) or six (“-6” units) SPDT (1 Form C) electro-mechanical relays (1 per counter) controlled in watchdog timer mode only. UL/CSA ratings are 1A @ 30VDC, 0.5A @110VDC, 0.5A @125VAC. Operate time is 1.5ms typical (3ms Maximum). Release time is 1ms typical (2ms Maximum). Note that 32-bit watchdog timers require two 16-bit counters and control the even-numbered counter’s relay (counter 2, 4, & 6 relay).

INDUSTRIAL I/O PACK COMPLIANCE

Specification.....This module meets or exceeds all written Industrial I/O Pack specifications per ANSI/VITA 4-1995, for Type I Modules.

Electrical/Mechanical Interface.....Single-Size IP Module.

IP Data Transfer Cycle Types Supported:

- Input/Output (IOSel*).....D16 or D08 (OE) R/W of I/O data.
- ID Read (IDSel*).....32 x 8 ID Space read on D0..D15.
- Interrupt Select (INTSel*).....8-bit word (D08) read of Interrupt Vector Register contents.

Access Times (8MHz Clock)……Read/Write Cycles require 1 wait state (375nS cycle) for accesses. The interrupt vector is served in 0 wait states (one 250ns cycle).

APPENDIX

CABLE: MODEL 5025-550-x (Non-Shielded)
MODEL 5025-551-x (Shielded)

Type: Flat Ribbon Cable, 50-wires (female connectors at both ends). The '-x' suffix designates the length in feet (12 feet maximum). Choose shielded or unshielded cable according to model number. The unshielded cable is recommended for digital I/O, while the shielded cable is recommended for optimum performance with precision analog I/O applications.

Application: Used to connect a Model 5025-552 termination panel to the AVME9630/9660 non-intelligent carrier board A-D connectors (both have 50-pin connectors). Also used for interface with the APC8610 carrier board.

Length: Last field of part number designates length in feet (user-specified, 12 feet maximum). It is recommended that this length be kept to a minimum to reduce noise and power loss.

Cable: 50-wire flat ribbon cable, 28 gage. Non-Shielded cable model uses Acromag Part 2002-211 (3M Type C3365/50 or equivalent). Shielded cable model uses Acromag Part 2002-261 (3M Type 3476/50 or equivalent).

Headers (Both Ends): 50-pin female header with strain relief. *Header* - Acromag Part 1004-512 (3M Type 3425-6600 or equivalent). *Strain Relief* - Acromag Part 1004-534 (3M Type 3448-3050 or equivalent).

Keying: Headers at both ends have polarizing key to prevent improper installation.

Schematic and Physical Attributes: For Non-Shielded cable model, see Drawing 4501-462. For Shielded cable model, see Drawing 4501-463.

Shipping Weight: 1.0 pound (0.5Kg) packaged.

TERMINATION PANEL: MODEL 5025-552

Type: Termination Panel For AVME9630/9660 Boards

Application: To connect field I/O signals to the Industrial I/O Pack (IP). *Termination Panel:* Acromag Part 4001-040 (Phoenix Contact Type FLKM 50). The 5025-552 termination panel facilitates the connection of up to 50 field I/O signals and connects to the AVME9630/9660 3U/6U non-intelligent carrier boards (A-D connectors only) via a flat ribbon cable (Model 5025-550-x or 5025-551-x). The A-D connectors on the carrier board connect the field I/O signals to the P2 connector on each of the Industrial I/O Pack modules. Field signals are accessed via screw terminal strips. The terminal strip markings on the termination panel (1-50) correspond to P2 (pins 1-50) on the Industrial I/O Pack (IP). Each Industrial I/O Pack (IP) has its own unique P2 pin assignments. Refer to the IP module manual for correct wiring connections to the termination panel.

Schematic and Physical Attributes: See Drawing 4501-464.

Field Wiring: 50-position terminal blocks with screw clamps. Wire range 12 to 26 AWG.

Connections to AVME9630/9660: P1, 50-pin male header with strain relief ejectors. Use Acromag 5025-550-x or 5025-551-x cable to connect panel to VME board. Keep cable as short as possible to reduce noise and power loss.

Mounting: Termination panel is snapped on the DIN mounting rail.

Printed Circuit Board: Military grade FR-4 epoxy glass circuit board, 0.063 inches thick.

Operating Temperature: -40°C to +100°C.

Storage Temperature: -40°C to +100°C.

Shipping Weight: 1.25 pounds (0.6kg) packaged.

TRANSITION MODULE: MODEL TRANS-GP

Type: Transition module for AVME9630/9660 boards.

Application: To repeat field I/O signals of IP modules A through D for rear exit from VME card cages. This module is available for use in card cages which provide rear exit for I/O connections via transition modules (transition modules can only be used in card cages specifically designed for them). It is a double-height (6U), single-slot module with front panel hardware adhering to the VMEbus mechanical dimensions, except for shorter printed circuit board depth. Connects to Acromag termination panel 5025-552 from the rear of the card cage, and to AVME9630/9660 boards within card cage, via flat 50-pin ribbon cable (cable Model 5025-550-X or 5025-551-X).

Schematic and Physical Attributes: See Drawing 4501-465.

Field Wiring: 100-pin header (male) connectors (3M 3433-D303 or equivalent) employing long ejector latches and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to Acromag termination panel 5025-552 from the rear of the card cage via flat 50-pin ribbon cable (cable Model 5025-550-X or 5025-551-X).

Connections to AVME9630/9660: 50-pin header (male) connectors (3M 3433-1302 or equivalent) employing long ejector latches and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to AVME9630/9660 boards within the card cage via flat 50-pin ribbon cable (cable Model 5025-550-X or 5025-551-X).

Mounting: Transition module is inserted into a 6U-size, single-width slot at the rear of the VMEbus card cage.

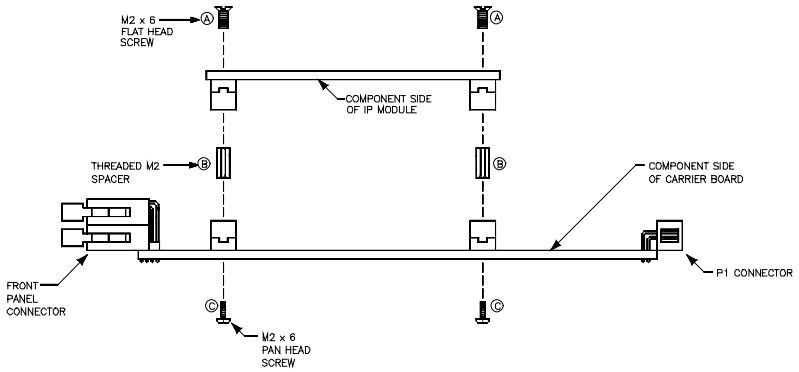
Printed Circuit Board: Six-layer, military-grade FR-4 epoxy glass circuit board, 0.063 inches thick.

Operating Temperature: -40°C to +85°C.

Storage Temperature: -55°C to +105°C.

Shipping Weight: 1.25 pounds (0.6Kg) packaged.

Notes:

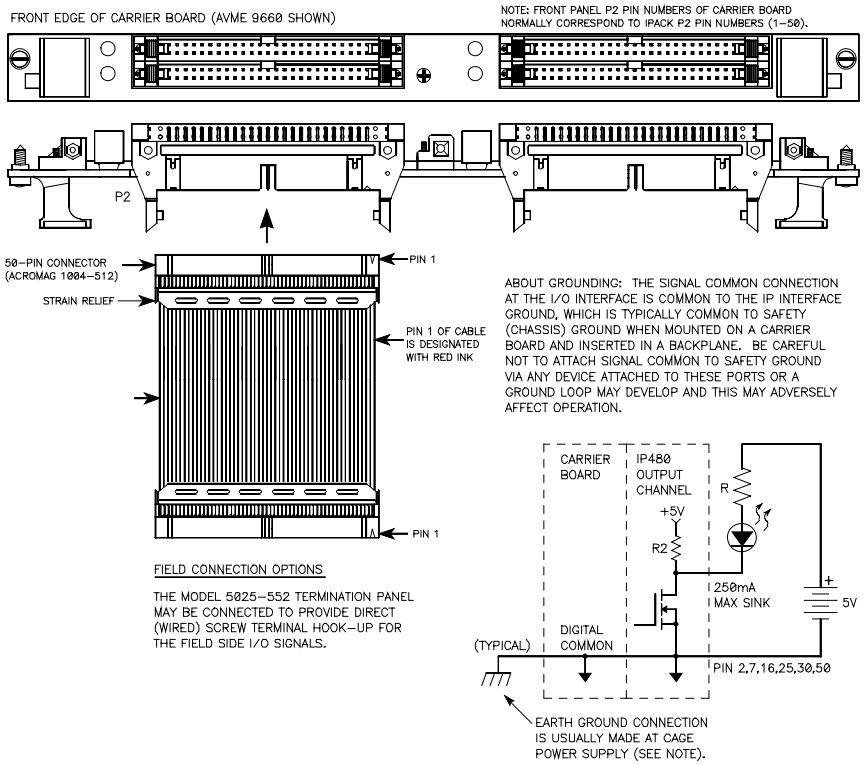


ASSEMBLY PROCEDURE:

1. THREADED SPACERS ARE PROVIDED IN TWO DIFFERENT LENGTHS. THE SHORTER LENGTH IS FOR USE WITH AVME 9630/9660 CARRIER BOARDS (SHOWN). CHECK YOUR CARRIER BOARD TO DETERMINE ITS REQUIREMENTS. MOUNTING HARDWARE PROVIDED MAY NOT BE COMPATIBLE WITH ALL TYPES OF CARRIER BOARDS.
2. INSERT FLAT HEAD SCREWS (ITEM A) THROUGH SOLDER SIDE OF IP MODULE AND INTO HEX SPACERS (ITEM B) AND TIGHTEN (4 PLACES) UNTIL HEX SPACER IS COMPLETELY SEATED.
3. CAREFULLY ALIGN IP MODULE TO CARRIER BOARD AND PRESS TOGETHER UNTIL CONNECTORS AND SPACERS ARE SEATED.
4. INSERT PAN HEAD SCREWS (ITEM C) THROUGH SOLDER SIDE OF CARRIER BOARD AND INTO HEX SPACERS (ITEM B) AND TIGHTEN (4 PLACES).

IP MODULE TO CARRIER BOARD MECHANICAL ASSEMBLY

4501-434B


FRONT EDGE OF CARRIER BOARD (AVME 9660 SHOWN)
NOTE: FRONT PANEL P2 PIN NUMBERS OF CARRIER BOARD NORMALLY CORRESPOND TO IPACK P2 PIN NUMBERS (1–50).
P2
50–PIN CONNECTOR
(ACROMAG 1004–512)
STRAIN RELIEF
PIN 1
PIN 1 OF CABLE
IS DESIGNATED
WITH RED INK
PIN 1
ABOUT GROUNDING: THE SIGNAL COMMON CONNECTION AT THE I/O INTERFACE IS COMMON TO THE IP INTERFACE GROUND, WHICH IS TYPICALLY COMMON TO SAFETY (CHASSIS) GROUND WHEN MOUNTED ON A CARRIER BOARD AND INSERTED IN A BACKPLANE. BE CAREFUL NOT TO ATTACH SIGNAL COMMON TO SAFETY GROUND VIA ANY DEVICE ATTACHED TO THESE PORTS OR A GROUND LOOP MAY DEVELOP AND THIS MAY ADVERSELY AFFECT OPERATION.
CARRIER
BOARD
IP480
OUTPUT
CHANNEL
+5V
R2
R
250mA
MAX SINK
5V
DIGITAL
COMMON
(TYPICAL)
PIN 2,7,16,25,30,50
EARTH GROUND CONNECTION
IS USUALLY MADE AT CAGE
POWER SUPPLY (SEE NOTE).

FIELD CONNECTION OPTIONS

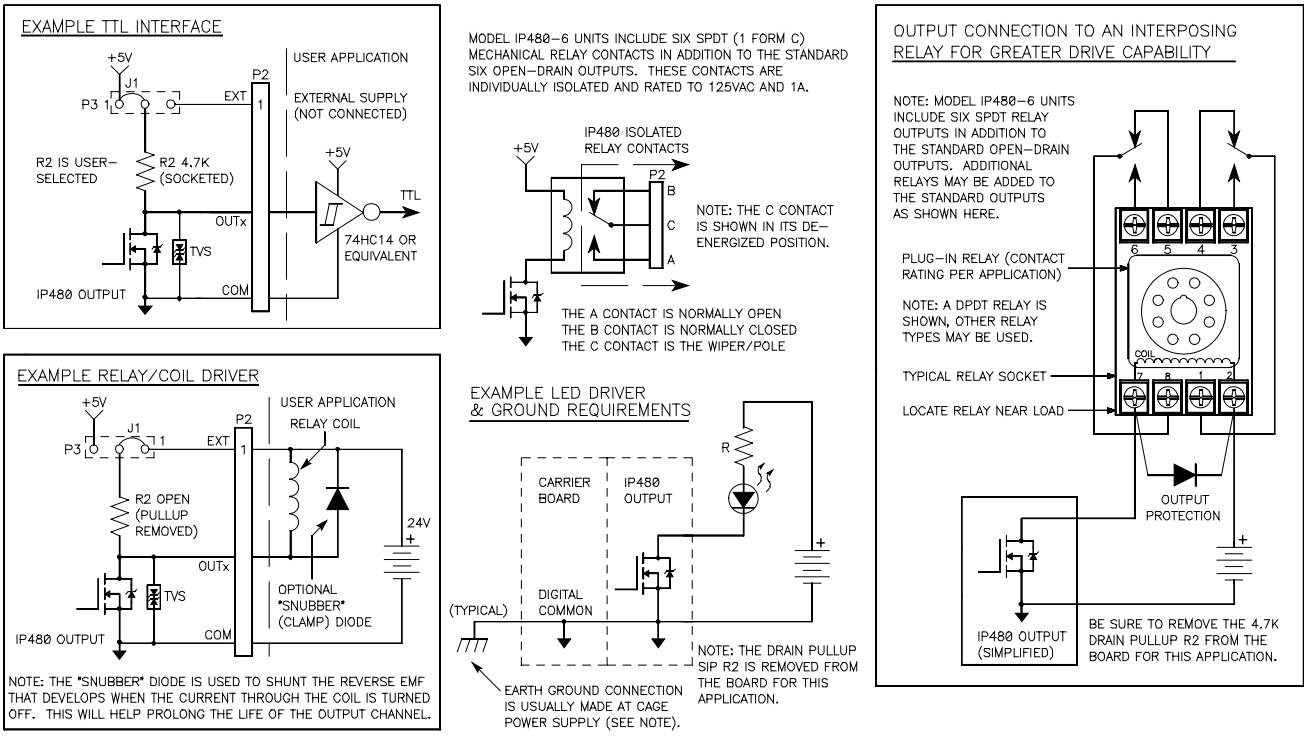
THE MODEL 5025–552 TERMINATION PANEL MAY BE CONNECTED TO PROVIDE DIRECT (WIRED) SCREW TERMINAL HOOK–UP FOR THE FIELD SIDE I/O SIGNALS.

P2 PIN ASSIGNMENTS

	I/O PIN	RIBBON CABLE/ P2 PIN NUMBER		I/O PIN	RIBBON CABLE/ P2 PIN NUMBER
	EXT SUPP	01			
	COM	02			
C	TRG1	03		RELAY 1	
N	INP1	04		1A (N.O.)	32
T	CLK1	05		1C	33
1	OUT1	06		1B (N.C.)	34
	COM	07			
C	TRG2	08		RELAY 2	
N	INP2	09		2A (N.O.)	35
T	CLK2	10		2C	36
2	OUT2	11		2B (N.C.)	37
C	TRG3	12		RELAY 3	
N	INP3	13		3A (N.O.)	38
T	CLK3	14		3C	39
3	OUT3	15		3B (N.C.)	40
	COM	16			
C	TRG4	17		RELAY 4	
N	INP4	18		4A (N.O.)	41
T	CLK4	19		4C	42
4	OUT4	20		4B (N.C.)	43
C	TRG5	21		RELAY 5	
N	INP5	22		5A (N.O.)	44
T	CLK5	23		5C	45
5	OUT5	24		5B (N.C.)	46
	COM	25			
C	TRG6	26		RELAY 6	
N	INP6	27		6A (N.O.)	47
T	CLK6	28		6C	48
6	OUT6	29		6B (N.C.)	49
	COM	30			
	NC	31		SHIELD	50

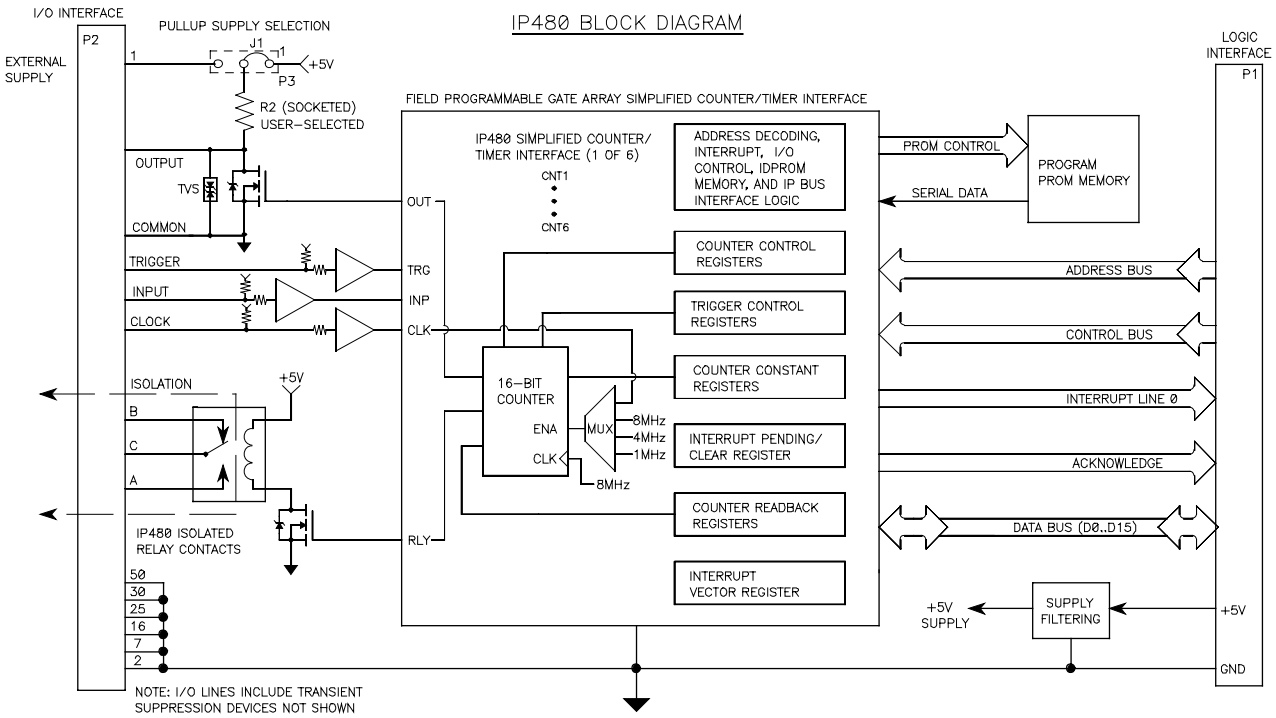
NOTE: ASSIGNMENTS SHOWN APPLY TO MODEL IP480–6. MODEL IP480–2 UNITS USE ONLY A THIRD OF THESE PINS (FOR 2 COUNTER/TIMERS).

4501-608A


EXAMPLE TTL INTERFACE
+5V
J1
P3
EXT
P2
USER APPLICATION
EXTERNAL SUPPLY
(NOT CONNECTED)
R2 IS USER-SELECTED
R2 4.7K
(SOCKETED)
OUTx
TVS
IP480 OUTPUT
COM
TTL
74HC14 OR
EQUIVALENT
MODEL IP480-6 UNITS INCLUDE SIX SPDT (1 FORM C) MECHANICAL RELAY CONTACTS IN ADDITION TO THE STANDARD SIX OPEN-DRAIN OUTPUTS. THESE CONTACTS ARE INDIVIDUALLY ISOLATED AND RATED TO 125VAC AND 1A.
IP480 ISOLATED
RELAY CONTACTS
NOTE: THE C CONTACT IS SHOWN IN ITS DE-ENERGIZED POSITION.
THE A CONTACT IS NORMALLY OPEN
THE B CONTACT IS NORMALLY CLOSED
THE C CONTACT IS THE WIPER/POLE
OUTPUT CONNECTION TO AN INTERPOSING RELAY FOR GREATER DRIVE CAPABILITY
NOTE: MODEL IP480-6 UNITS INCLUDE SIX SPDT RELAY OUTPUTS IN ADDITION TO THE STANDARD OPEN-DRAIN OUTPUTS. ADDITIONAL RELAYS MAY BE ADDED TO THE STANDARD OUTPUTS AS SHOWN HERE.
PLUG-IN RELAY (CONTACT RATING PER APPLICATION)
NOTE: A DPDT RELAY IS SHOWN, OTHER RELAY TYPES MAY BE USED.
TYPICAL RELAY SOCKET
LOCATE RELAY NEAR LOAD
COIL
OUTPUT PROTECTION
IP480 OUTPUT (SIMPLIFIED)
BE SURE TO REMOVE THE 4.7K DRAIN PULLUP R2 FROM THE BOARD FOR THIS APPLICATION.
EXAMPLE RELAY/COIL DRIVER
USER APPLICATION
RELAY COIL
R2 OPEN (PULLUP REMOVED)
24V
OPTIONAL "SNUBBER" (CLAMP) DIODE
NOTE: THE "SNUBBER" DIODE IS USED TO SHUNT THE REVERSE EMF THAT DEVELOPS WHEN THE CURRENT THROUGH THE COIL IS TURNED OFF. THIS WILL HELP PROLONG THE LIFE OF THE OUTPUT CHANNEL.
EXAMPLE LED DRIVER & GROUND REQUIREMENTS
CARRIER BOARD
IP480 OUTPUT
DIGITAL COMMON
(TYPICAL)
R
NOTE: THE DRAIN PULLUP SIP R2 IS REMOVED FROM THE BOARD FOR THIS APPLICATION.
EARTH GROUND CONNECTION IS USUALLY MADE AT CAGE POWER SUPPLY (SEE NOTE).
NOTE: MULTIPLE EARTH GROUNDS CAUSE GROUND LOOPS AND MUST BE AVOIDED.

IP480 EXAMPLE OUTPUT CONNECTIONS

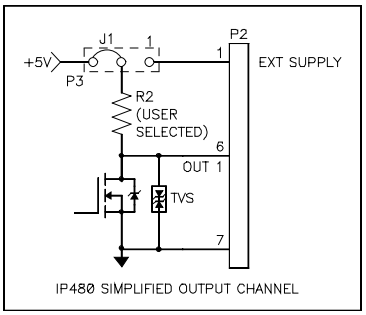
4501-611



4501-609A

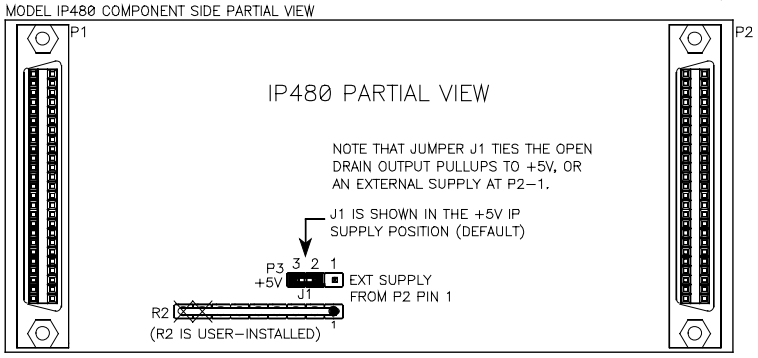
IP480 EXTERNAL SUPPLY JUMPER AND OUTPUT PULLUP RESISTOR LOCATION DRAWING

OUTPUT PULLUP RESISTOR SIP R2 IS A GROUP OF 6, 7, OR 8 RESISTORS WITH A COMMON PIN (PIN 1 OF 9 PINS). THE PIN 1 POSITION IS IDENTIFIED BY A DOT. PIN 1 IS TIED TO THE SELECTED SUPPLY (+5V OF BOARD OR THE EXT SUPPLY PIN 1 OF P2).



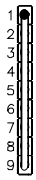
IP480 SIMPLIFIED OUTPUT CHANNEL

MODEL IP480 COMPONENT SIDE PARTIAL VIEW


P1
P2
IP480 PARTIAL VIEW
NOTE THAT JUMPER J1 TIES THE OPEN DRAIN OUTPUT PULLUPS TO +5V, OR AN EXTERNAL SUPPLY AT P2–1.
J1 IS SHOWN IN THE +5V IP SUPPLY POSITION (DEFAULT)
P3 3 2 1
+5V
J1
EXT SUPPLY FROM P2 PIN 1
R2
1
(R2 IS USER–INSTALLED)

RESISTOR SIP R2 IS MOUNTED IN SOCKET X1 AND MAY BE CHANGED OR REMOVED IF REQUIRED.

RESISTOR SIPS ARE DIVIDED AS SHOWN



1 COMMON PIN
2 A (OUT 1)
3 B (OUT 2)
4 C (OUT 3)
5 D (OUT 4)
6 E (OUT 5)
7 F (OUT 6)
8 G (NO CONNECTION)
9 H (NO CONNECTION)

DETAIL "A"

NOTE THAT THE LAST TWO SIP RESISTOR PINS ARE NOT CONNECTED.

THE COMMON PIN OF RESISTOR SIP R2 IS CONNECTED TO THE ACTIVE SUPPLY (+5V OF BOARD OR EXT SUPPLY PIN P2–1) AS PROGRAMMED VIA P3 JUMPER J1.

OUTPUT PIN NUMBERS

OUTPUT	P2 PIN	SIP R2 PIN
OUT 1	6	2
OUT 2	11	3
OUT 3	15	4
OUT 4	20	5
OUT 5	24	6
OUT 6	29	7

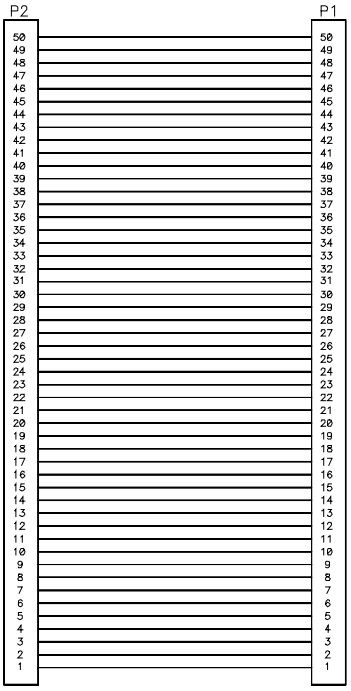
MODULE IS SHIPPED WITH A 4.7K INSTALLED, AND 470 OHM SIP RESISTOR WHICH IS PACKED SEPARATELY. INSTALL THIS RESISTOR FOR PROPER OUTPUT OPERATION.

NOTES CONCERNING OUTPUT PULLUP RESISTOR SIP R2 AND JUMPER J1:

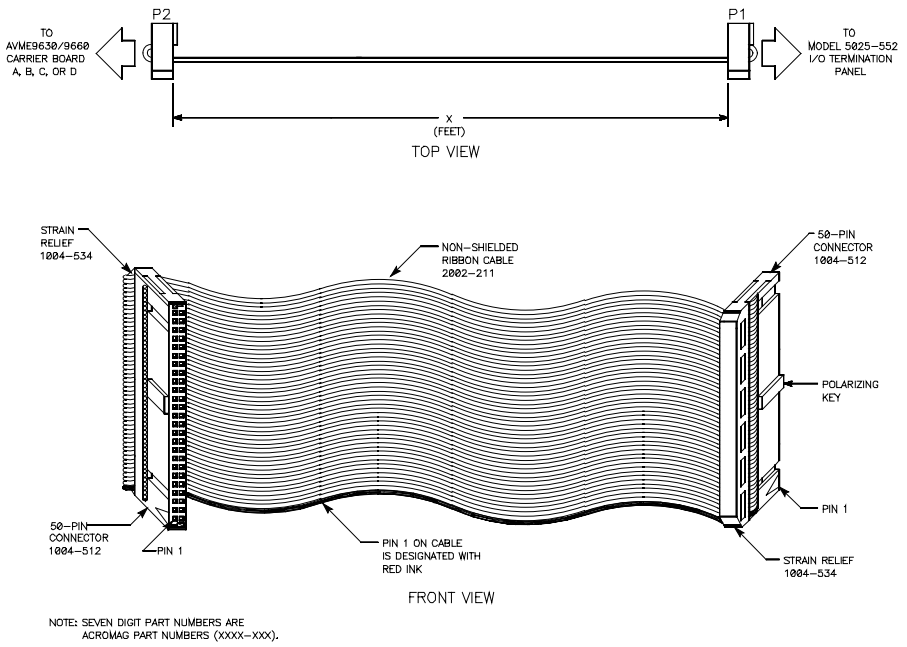
1. COUNTER/TIMER OUTPUTS ARE THE OPEN DRAINS OF MOSFETS AND INCLUDE PULLUP RESISTORS TO +5V OR THE EXTERNAL SUPPLY PIN. THE PULLUP SUPPLY FOR THESE OUPUTS IS PROGRAMMED VIA JUMPER J1. SELECT THE +5V IP SUPPLY OR AN EXTERNAL SUPPLY CONNECTED TO PIN 1 OF P2. FROM THE FACTORY, J1 IS INSTALLED BETWEEN P3 PINS 2 & 3 TO SELECT THE USE OF THE IP +5V SUPPLY FOR PULLUP OF THE OUTPUT DRAINS.
2. PULLUP RESISTORS MUST BE INSTALLED FOR PROPER OUTPUT OPERATION. TWO RESISTOR SIPS ARE PROVIDED. A 4.7K OHM RESISTOR SIP IS INSTALLED AND A 470 OHM RESISTOR SIP IS PACKED SEPARATELY FROM THE MODULE. THIS RESISTOR SIP R2 IS INSTALLED IN SOCKET X1 FOR EASY REPLACEMENT AND REMOVAL. ADJUST THIS VALUE FOR DIFFERENT SUPPLY LEVELS AND LOAD REQUIREMENTS. REDUCING THIS VALUE WILL ALSO DECREASE THE OUTPUT RESPONSE TIME. BE CAREFUL NOT TO EXCEED 0.15 WATTS OF POWER PER RESISTOR. REMOVE SIP R2 AND USE AN EXTERNAL PULLUP FOR GREATER DRIVE CAPABILITY. OUTPUTS MUST BE LIMITED TO VOLTAGES LESS THAN 60V AND CURRENTS BELOW 250mA WITH R2 REMOVED.

4501–610B

Notes:

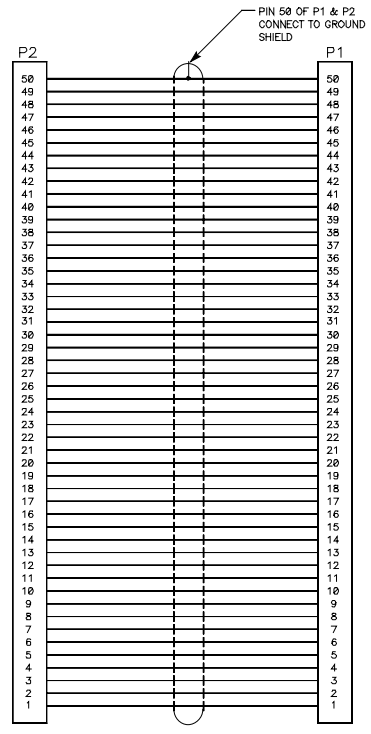


MODEL 5025–550–x SCHEMATIC

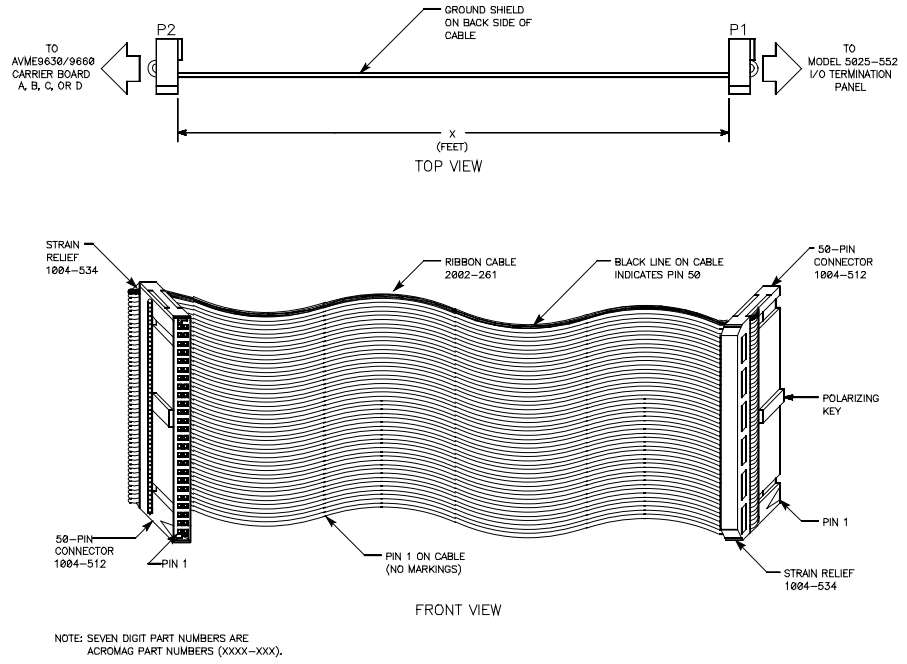


MODEL 5025–550–x SIGNAL CABLE, NON–SHIELDED

4501-462A

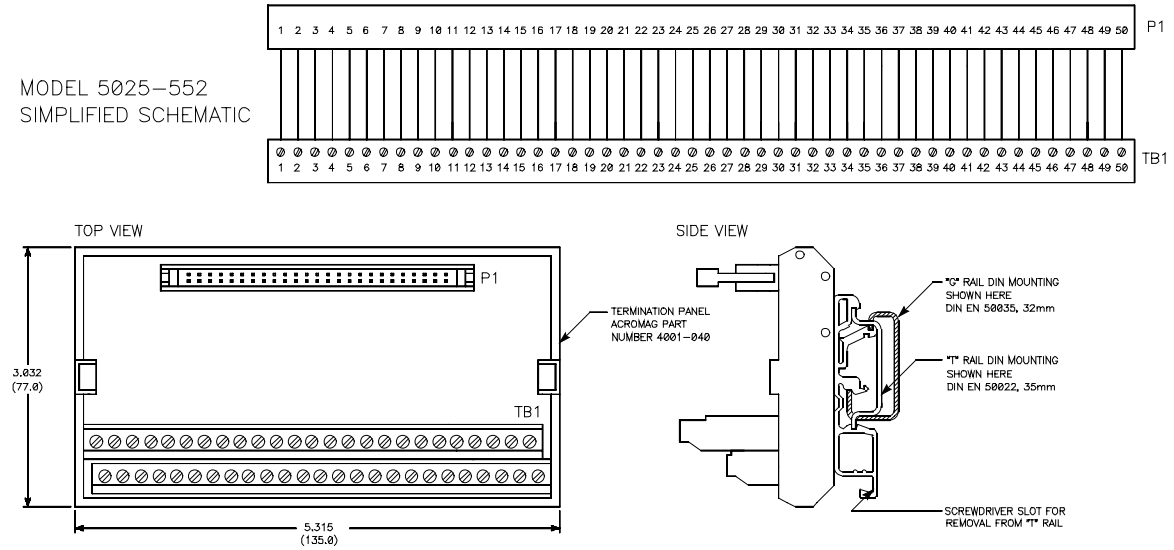


MODEL 5025–551–x SCHEMATIC

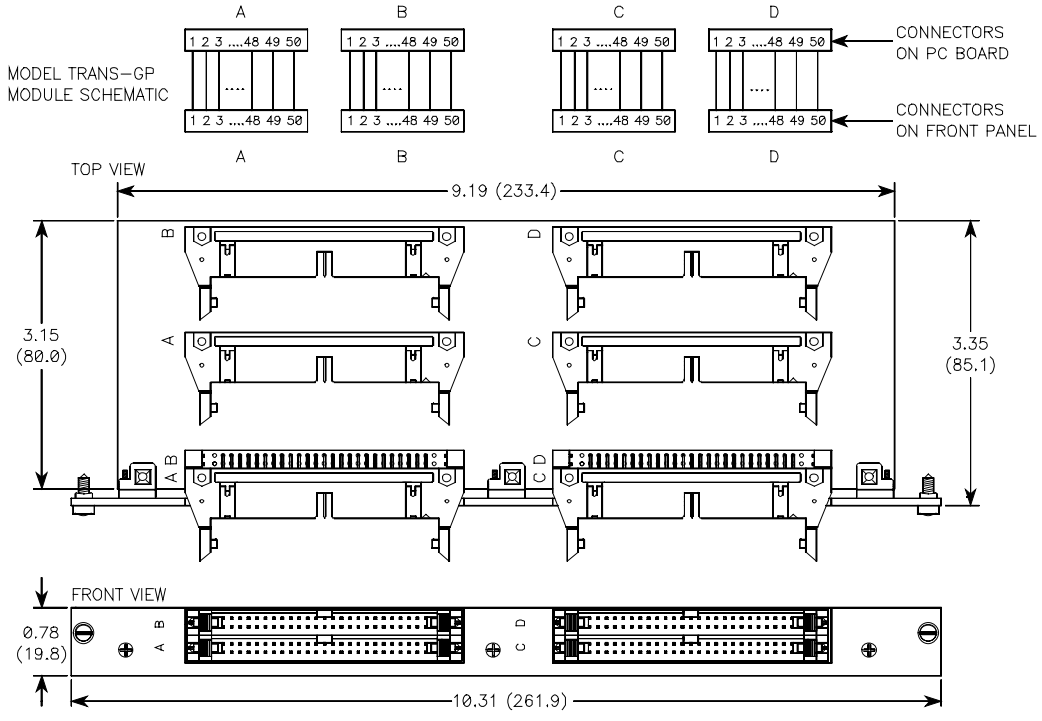


MODEL 5025–551–x SIGNAL CABLE, SHIELDED

4501-463A



4501-464A



4501-465A